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1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.

2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.

3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

J41 MLB SCHEMATIC 6.6.0

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Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-9795	1	SCHEM,MLB,J41	SCH	CRITICAL	
820-3435	1	PCBF,MLB,J41	PCB	CRITICAL	

DRAWING

TITLE-MLB

ABREV-DRAWING

DATE: 2013/09/13 10:10 AM

PRODUCT SAFETY REQUIREMENTS:

PCB, UL RECOGNIZED, MIN. 130-C TEMP. RATING AND V-0 FLAME RATING PER UL 796 & UL 94.

PCB TO BE SILK-SCREENED WITH UL/CUL RECOGNITION MARK, MANUFACTURER'S UL FILE NUMBER, UL PCB MATERIAL DESIGNATION, 130-C TEMP. RATING AND V-0 FLAME RATING.

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BOM Groups

BOM GROUP	BOM OPTIONS
MLB_COMMON	ALTERNATE,COMMON,MLB_MISC,MLB_DEBUG:ENG,MLB_PROGPARTS
MLB_MISC	PP5V5_DCIN:NO,TETHV:P15V,EDP,CAM_XTAL:NO,CAM_WAKE:NO,APCLKRQ:ISOL,TPAD_INTWAKE:SHARED,USB_PWR:S3,SD_ON_MLB,VCORE_FETS
MLB_DEVEL:ENG	ALTERNATE,BKLT:ENG,XDP_CONN,DDRVREF_DAC,S0PGOOD_ISL,DBGLED,ISNS:ENG
MLB_DEVEL:PVT	XDP_CONN
MLB_DEBUG:ENG	DEVEL_BOM,XDP,LPCPLUS
MLB_DEBUG:PVT	DEVEL_BOM,BKLT:PROD,XDP,LPCPLUS,ISNS:PROD
MLB_DEBUG:PROD	BKLT:PROD,LPCPLUS,XDP,ISNS:PROD

Current Sensor Configuration

BOM GROUP	BOM OPTIONS
ISNS : ENG	CPU_HS_1SNS : YES, CP0VR_1SNS : YES, DRAM_1SNS : YES, P1V05_1SNS : YES, AIRPORT_1SNS : YES, SSD_1SNS : YES, LCDBLT_1SNS : YES, P3V3S5_1SNS : YES, JY3S0_1SNS : YES, OTHER_HS_1SNS : YES, CAM_1SNS : YES, CPUCOR_1SNS : YES, PANEL_1SNS : YES
ISNS : PROD	CPU_HS_1SNS : YES, CP0VR_1SNS : YES, DRAM_1SNS : YES, P1V05_1SNS : NO, AIRPORT_1SNS : NO, SSD_1SNS : YES, LCDBLT_1SNS : NO, P3V3S5_1SNS : NO, JY3S0_1SNS : NO, OTHER_HS_1SNS : NO, CAM_1SNS : NO, CPUCOR_1SNS : NO, PANEL_1SNS : NO

CPU DRAM SPD Straps

BOM GROUP	BOM OPTIONS
DDR3:HYNIX_4GB	RAMCFG0:L, RAMCFG1:L, RAMCFG2:L, RAMCFG3:L, DRAM_TYPE:HYNIX_4GB
DDR3:HYNIX_8GB	RAMCFG0:L, RAMCFG1:L, RAMCFG2:H, RAMCFG3:L, DRAM_TYPE:HYNIX_8GB
DDR3:SAMSUNG_4GB	RAMCFG0:L, RAMCFG1:H, RAMCFG2:L, RAMCFG3:L, DRAM_TYPE:SAMSUNG_4GB
DDR3:SAMSUNG_8GB	RAMCFG0:L, RAMCFG1:H, RAMCFG2:H, RAMCFG3:L, DRAM_TYPE:SAMSUNG_8GB
DDR3:ELPIDA_4GB	RAMCFG0:H, RAMCFG1:H, RAMCFG2:L, RAMCFG3:L, DRAM_TYPE:ELPIDA_4GB
DDR3:ELPIDA_8GB	RAMCFG0:H, RAMCFG1:H, RAMCFG2:H, RAMCFG3:L, DRAM_TYPE:ELPIDA_8GB
DDR3:MICRON_4GB	RAMCFG0:H, RAMCFG1:L, RAMCFG2:L, RAMCFG3:L, DRAM_TYPE:MICRON_4GB

Programmable Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S0865	1	EEPROM, 256KBIT, SPI, 5MHZ, 1.8V, 2X3QFN	U2890	CRITICAL	TBTR0M: BLANK
341S3802	1	IC, EEPROM, C/R (V23.4) EVT, J41/J41	U2890	CRITICAL	TBTR0M: PROG
338S1159	1	IC, SMC12-A3, 40MHZ/50DIMIPS MCU, 9X9, 157BGA	U5000	CRITICAL	SMC: BLANK
335S0809	1	64 MBIT SPI SERIAL DUAL I/O FLASH, 8X6X0.8	U6100	CRITICAL	BOOTROM_MAC: BLANK
335S0803	1	64 MBIT SPI SERIAL DUAL I/O FLASH, 8X6X0.8	U6100	CRITICAL	BOOTROM_NUM: BLANK
341S3809	1	IC, EFI ROM (V0071) DVT, J41/J43	U6100	CRITICAL	BOOTROM: PROG

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S4525	1	HSW,SR16M,PRQ,C0,1,3,15W,2+3,1,0,3M,BGA	U0500	CRITICAL	CPU:1.3GHZ
337S4526	1	HSW,SR16L,PRQ,C0,1,4,15W,2+3,1,1,3M,BGA	U0500	CRITICAL	CPU:1.4GHZ
337S4528	1	HSW,SR16M,PRQ,C0,1,7,15W,2+3,1,1,4M,BGA	U0500	CRITICAL	CPU:1.7GHZ
338S1113	1	IC,TBT,CR-4C,B1,PRQ,C10,286,12X12 FC-CSP	U2800	CRITICAL	
338S1186	1	IC,BCM15700A2,S2 PCIE CAMERA PROCESSOR	U3900	CRITICAL	
607-6811	1	ASSEMBLY,SUBASSY,PCBA,HALL EFFECT,K99	J6955	CRITICAL	J41_MLB
946-3892	1	J11/J13 MLB DYNAM ADHESIVE 29993-SC 0.40	GLUE	CRITICAL	
825-7670	1	LABEL,TEXT,MLB,K21/K78	LABEL		
376S0964	2	MOSFET,N-CH,25V,30A,9.6M,8P 3.3X3.3 DFN	Q7310,Q7320	CRITICAL	VCORE_FET:REN
376S1104	2	MOSFET,N-CH,25V,30A,6.1M,8P 3.3X3.3 DFN	Q7311,Q7321	CRITICAL	VCORE_FET:REN
376S1173	2	MOSFET,N-CH,30V,15.3A,12M,8P 3.3X3.3 DFN	Q7310,Q7320	CRITICAL	VCORE_FET:VSHY
376S1174	2	MOSFET,N-CH,30V,22A,6.0M,8P 3.3X3.3 DFN	Q7311,Q7321	CRITICAL	VCORE_FET:VSHY
900-0090	1		SOLDERPASTE	CRITICAL	

DRAM Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S0677	4	IC,SDRAM,8Gb,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	DRAM_TYPE:HYNIX_4Gb
333S0681	4	IC,SDRAM,16Gb,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	DRAM_TYPE:HYNIX_8Gb
333S0676	4	IC,SDRAM,8Gb,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	DRAM_TYPE:SAMSUNG_4Gb
333S0680	4	IC,SDRAM,16Gb,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	DRAM_TYPE:SAMSUNG_8Gb
333S0678	4	IC,SDRAM,8Gb,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	DRAM_TYPE:ELPIDA_4Gb
333S0666	4	IC,SDRAM,16Gb,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	DRAM_TYPE:ELPIDA_8Gb
333S0679	4	IC,SDRAM,8Gb,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	DRAM_TYPE:MICRON_4Gb

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S1032	376S0855		ALL	Toshiba alt for Diodes dual
376S1129	376S0855		ALL	NEK alt for Diodes dual
376S1089	376S1128		ALL	NEK alt for Diodes single
138S0684	138S0660		ALL	Murata alt to Taiyo Yuden
138S0703	138S0648		ALL	Murata alt to Taiyo Yuden
152S0586	152S1301		ALL	Dale/Vishay alt to Cytotec
372S0186	372S0185		ALL	NEK alt to Diodes
197S0479	197S0478		ALL	200uW Epcos alt to NEK
376S1053	376S0604		ALL	Diodes alt to Fairchild
371S0713	371S0558		ALL	Diodes alt to ST Micro
128S0371	128S0376		ALL	Kemet alt to Sanyo
128S0394	128S0415		ALL	NEC alt to Sanyo
152S1821	152S1757		ALL	Cytotec alt to NEC
197S0480	197S0343		ALL	NEK crystal alt to TSC
197S0481	197S0343		ALL	Epcos crystal alt to TSC
107S0254	107S0241		ALL	Cytotec sense R alt to TFF
353S3452	353S1286		ALL	Maxim alt to Microchip
128S0386	128S0284		ALL	Kemet alt to Sanyo
128S0397	128S0325		ALL	Kemet alt to Sanyo
377S0155	377S0104		ALL	OnSemi alt to Infineon
128S0398	128S0220		ALL	Kemet alt to Sanyo
197S0542	197S0544		ALL	NEK alt to TSC
197S0545	197S0544		ALL	Epcos alt to TSC
138S0681	138S0638		ALL	Taiyo alt to Samsung
138S0841	138S0638		ALL	Murata alt to Samsung
376S1180	376S0761		ALL	Remesas alt to Vishay
152S1876	152S1804		ALL	TDK alt to Toko
107S0255	107S0240		ALL	Cytotec alt to TFF
107S0250	107S0248		ALL	Cytotec alt to TFF

CPU DRAM CFG Chart

VENDOR	CFG 1	CFG 0
HYNIX	0	0
SAMSUNG	1	0
MICRON	0	1
ELPIDA	1	1

SIZE	CFG 2
4GB	0
8GB	1

DIE REV	CFG 3
A	0
B	1

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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
639-4118	PCBA,MLB,BEST,HY 4GB,J41:	MLB_CMNPTS,CPU:1.7GHZ,DDR3:HYNIX_4GB
639-4274	PCBA,MLB,BEST,HY 8GB,J41	MLB_CMNPTS,CPU:1.7GHZ,DDR3:HYNIX_8GB
639-4275	PCBA,MLB,BEST,EL 4GB,J41	MLB_CMNPTS,CPU:1.7GHZ,DDR3:ELPIDA_4GB
639-4276	PCBA,MLB,BEST,EL 8GB,J41	MLB_CMNPTS,CPU:1.7GHZ,DDR3:ELPIDA_8GB
639-4702	PCBA,MLB,BEST,MI 4GB,J41	MLB_CMNPTS,CPU:1.7GHZ,DDR3:MICRON_4GB
639-4434	PCBA,MLB,BETTER,HY 4GB,J41	MLB_CMNPTS,CPU:1.3GHZ,DDR3:HYNIX_4GB
639-4435	PCBA,MLB,BETTER,HY 8GB,J41	MLB_CMNPTS,CPU:1.3GHZ,DDR3:HYNIX_8GB
639-4436	PCBA,MLB,BETTER,EL 4GB,J41	MLB_CMNPTS,CPU:1.3GHZ,DDR3:ELPIDA_4GB
639-4437	PCBA,MLB,BETTER,EL 8GB,J41	MLB_CMNPTS,CPU:1.3GHZ,DDR3:ELPIDA_8GB
639-4703	PCBA,MLB,BETTER,MI 4GB,J41	MLB_CMNPTS,CPU:1.3GHZ,DDR3:MICRON_4GB
685-0024	CMN PTS,PCBA,MLB,J41	MLB_COMMON,J41_MLB
985-0017	J41 MLB DEVELOPMENT BOM	MLB_DEVEL:ENG
685-0062	VCORE FET,REN,J41	VCORE_FET:REN
685-0063	VCORE FET,VSHY,J41	VCORE_FET:VSHY

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
685-0062	685-0063		ALL	Semsaas alt to Vishay
333S0704	333S0700		ALL	Elpida CAM CHAM alt to Hynix

BOM Groups

BOM GROUP	BOM OPTIONS
MLB_PROGPARTS	BOOTROM:PROG,SMC:PROG,TBTROM:PROG

Programmable Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
341S3757	1	IC,SMC-A3 SCPL,EXT,V22.12A18,PROTO 1,J41	U5000	CRITICAL	SMC:PROG

Sub-BOMs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
985-0017	1	J41 MLB DEVELOPMENT BOM	DEVEL	CRITICAL	DEVEL_BOM
685-0024	1	CMN PTS,PCBA,MLB,J41	CMNPTS	CRITICAL	MLB_CMNPTS
685-0063	1	VCORE FET,VSHY,J41	VCOREFETS	CRITICAL	VCORE_FETS

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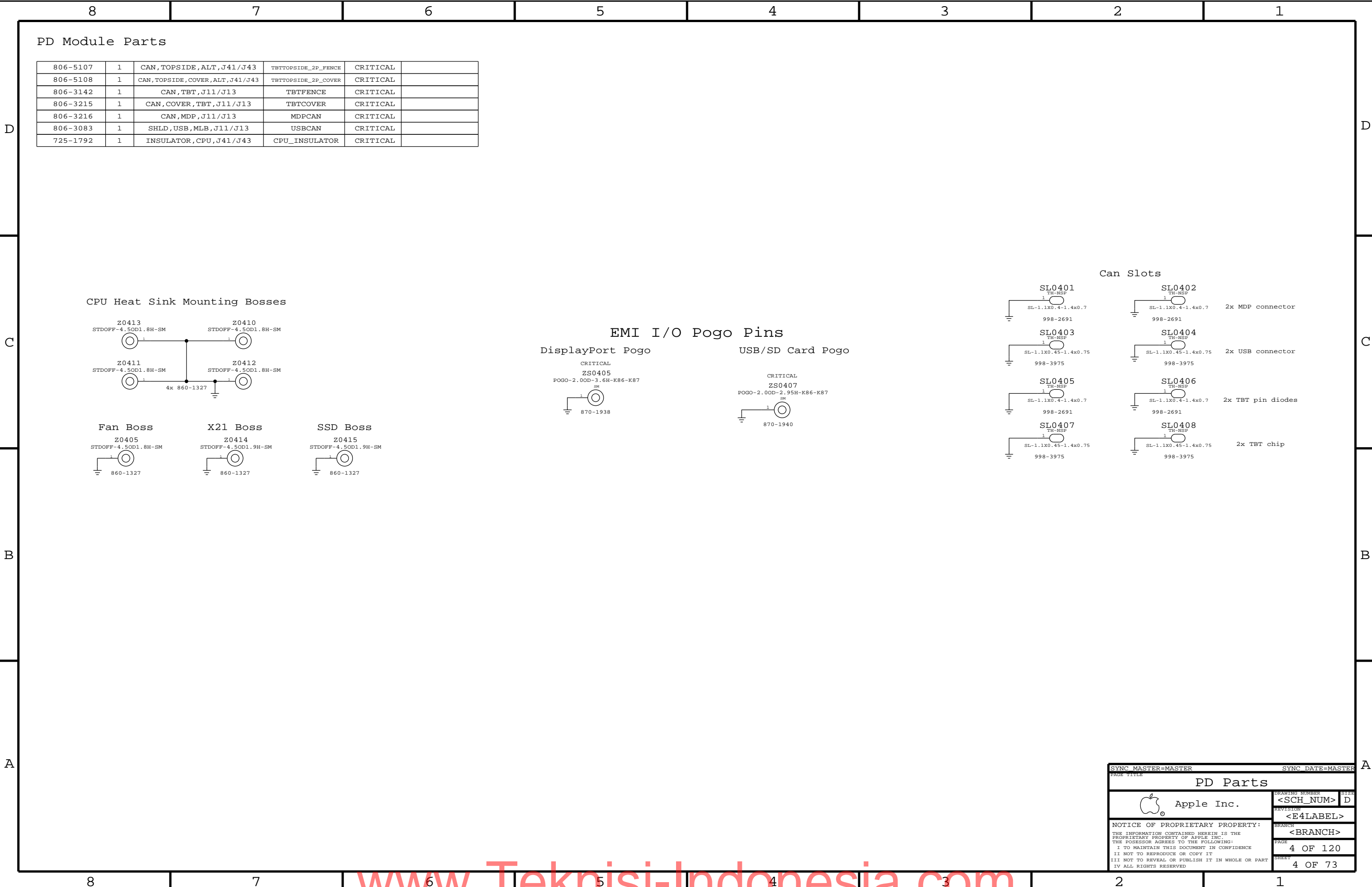
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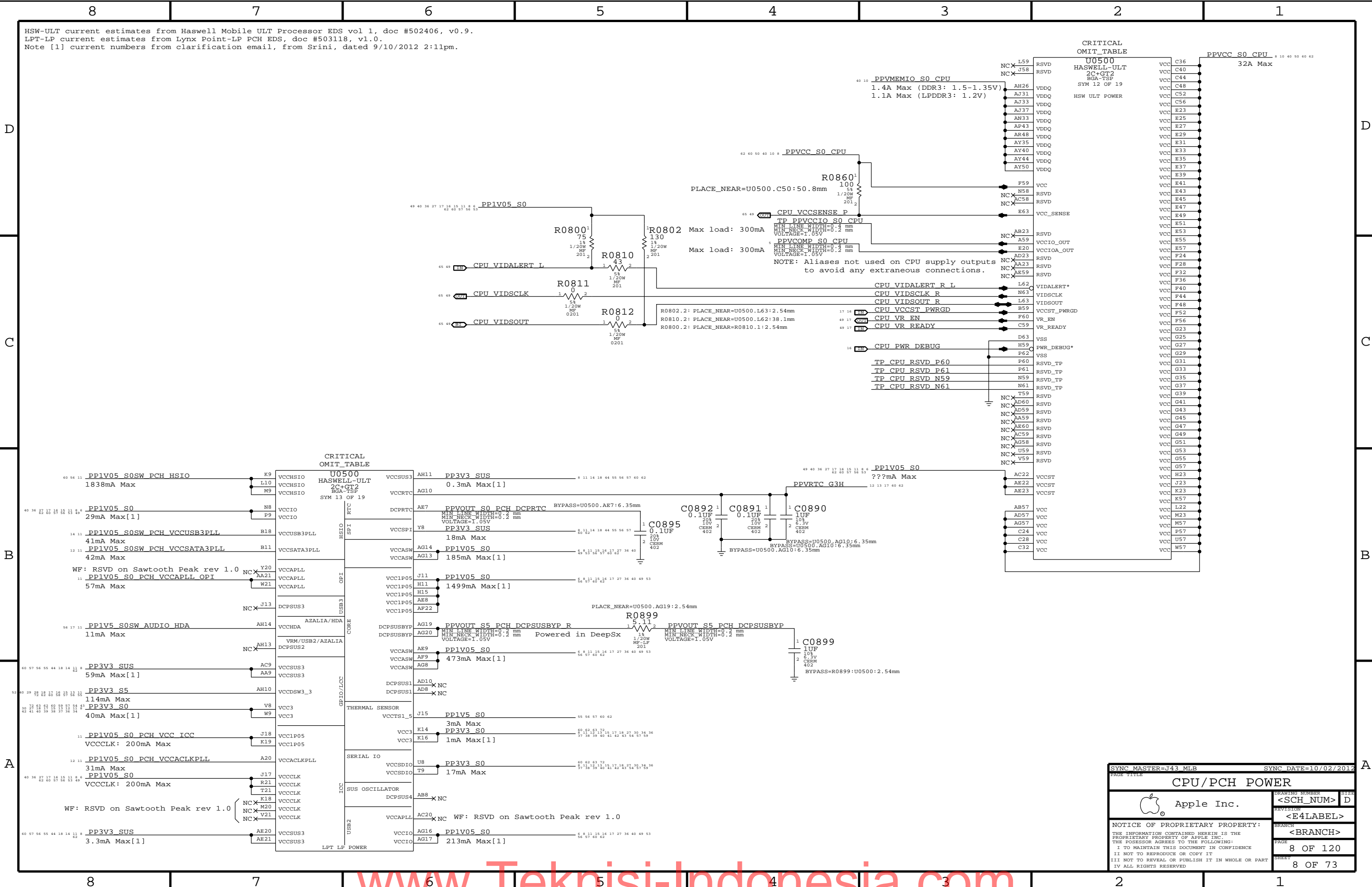
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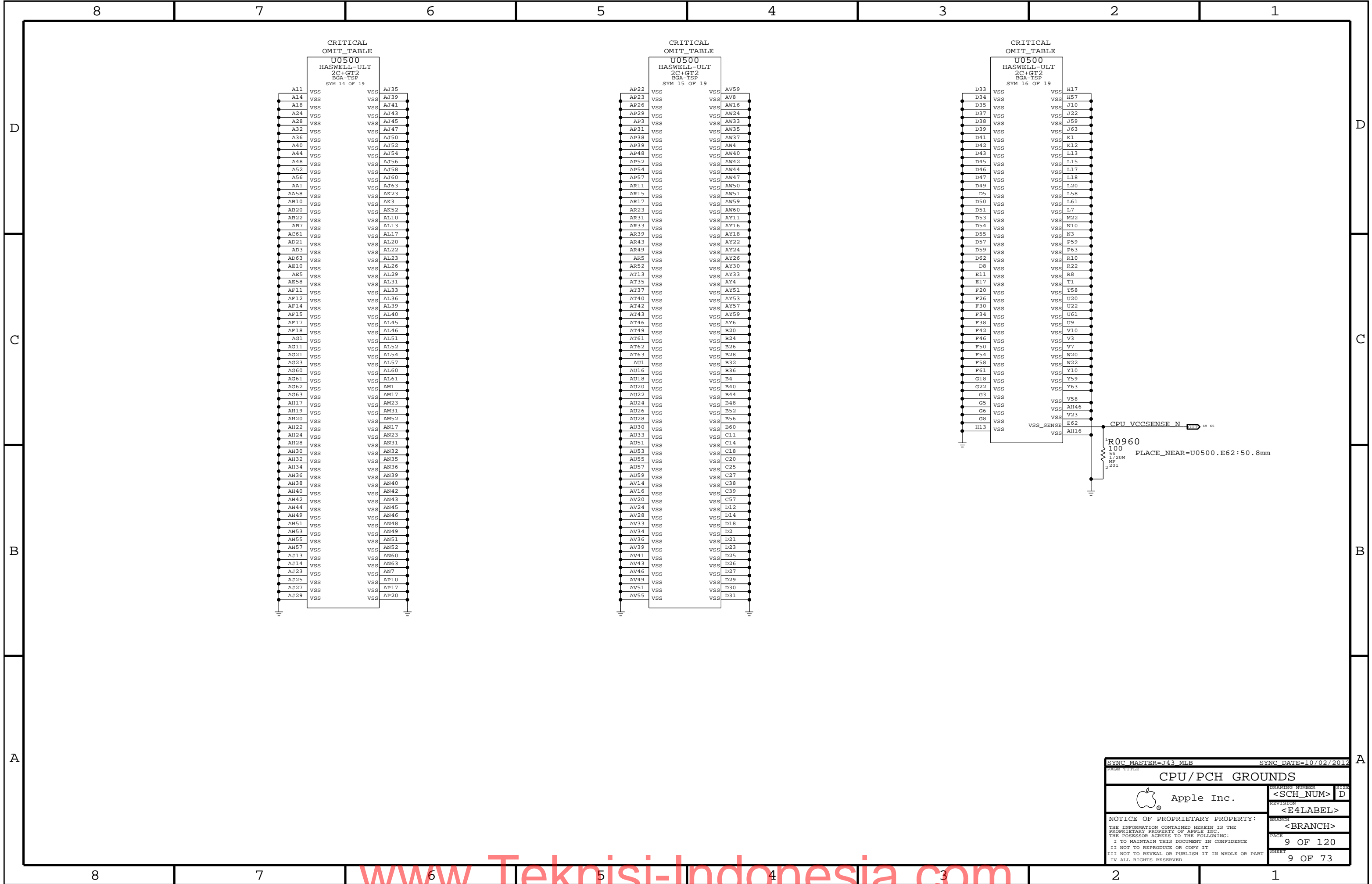
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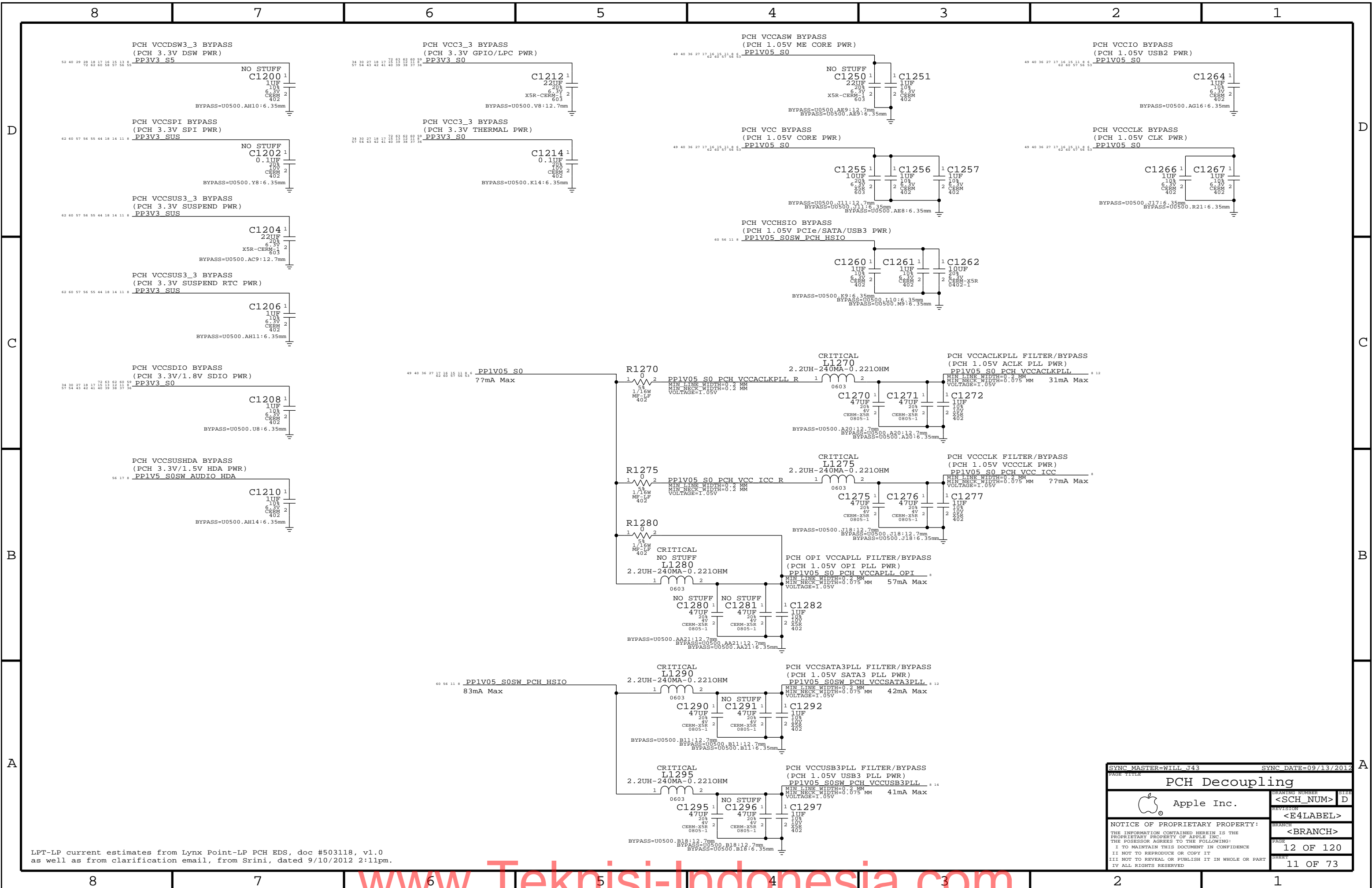
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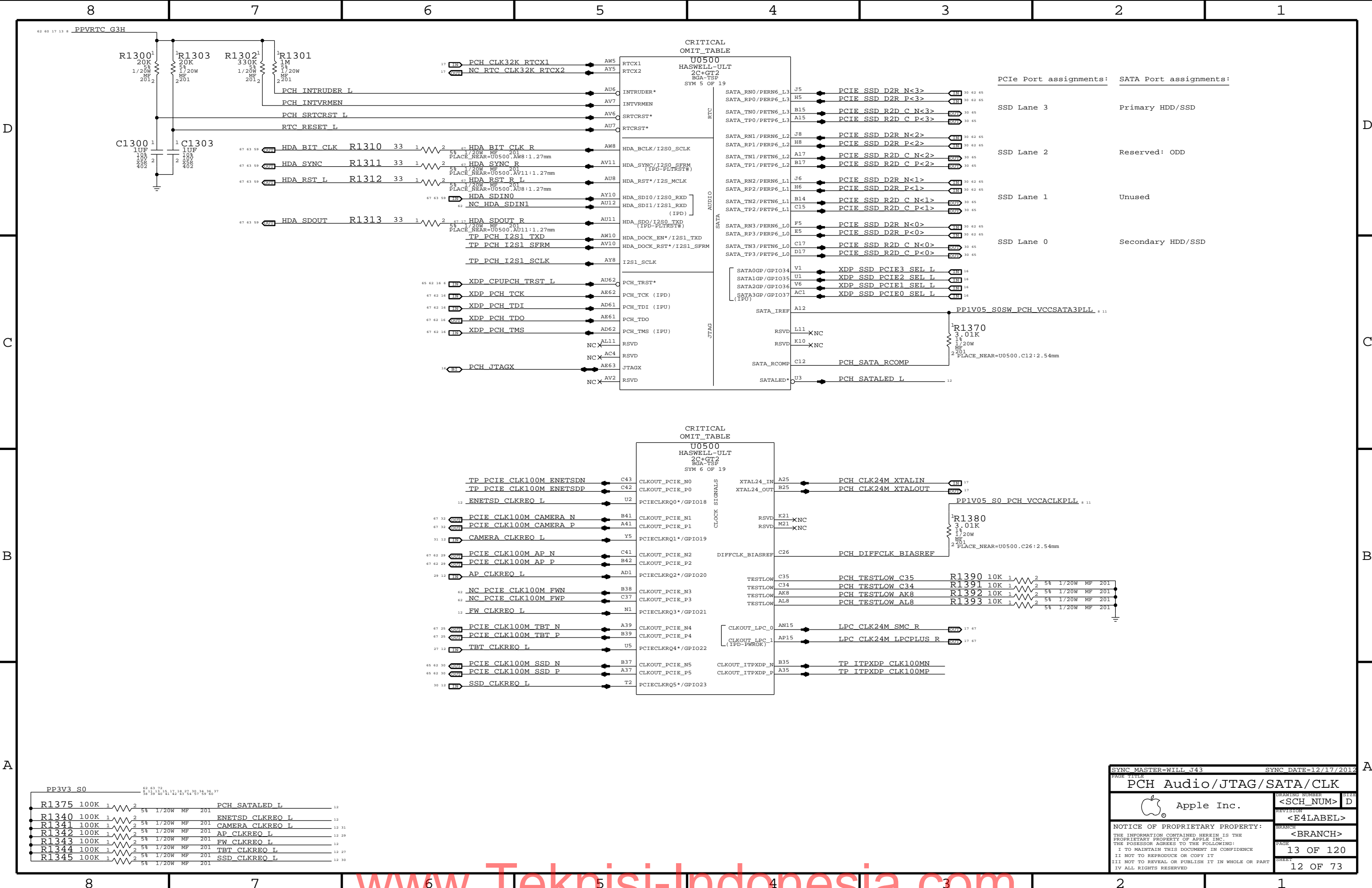
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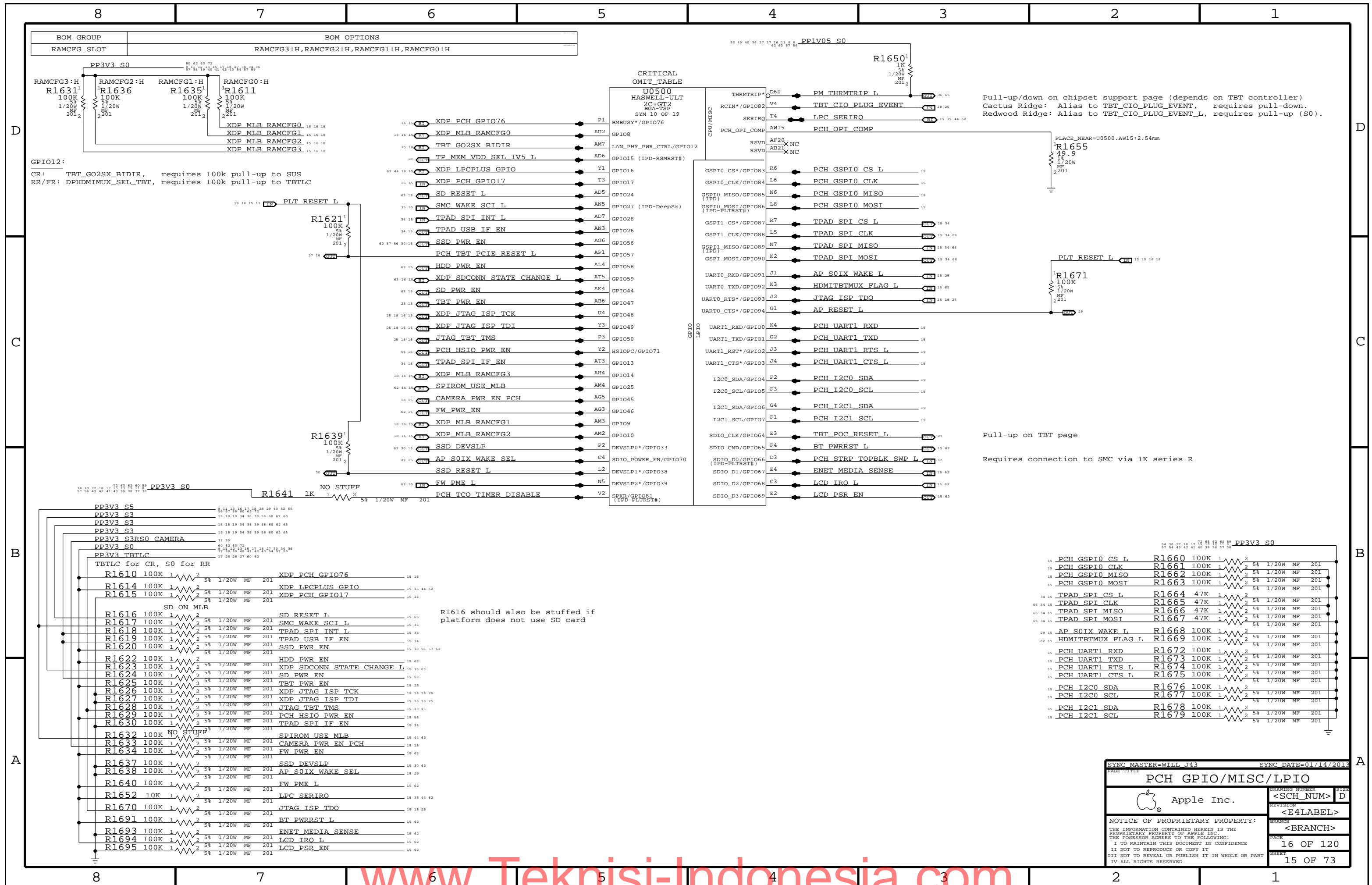


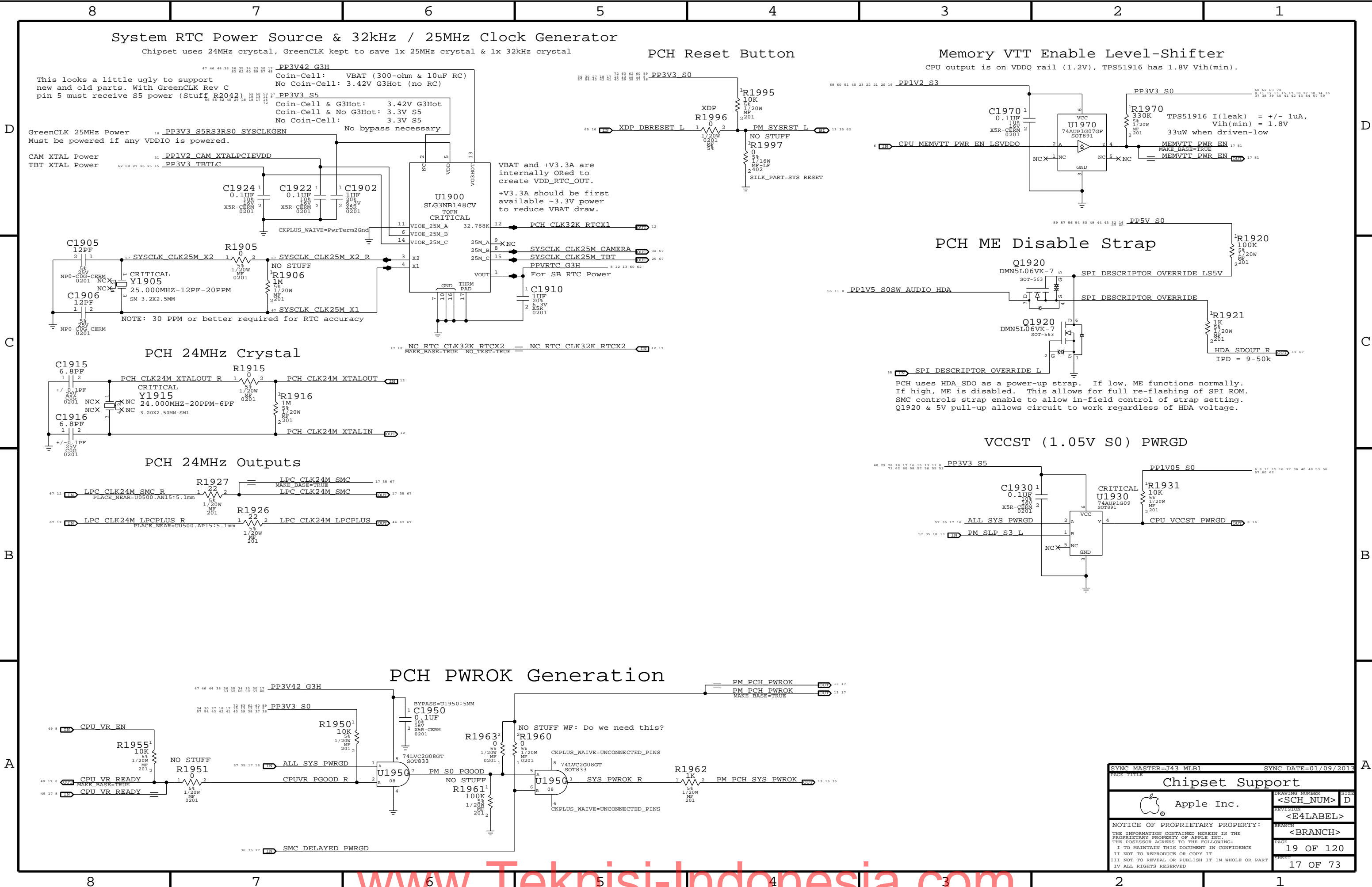


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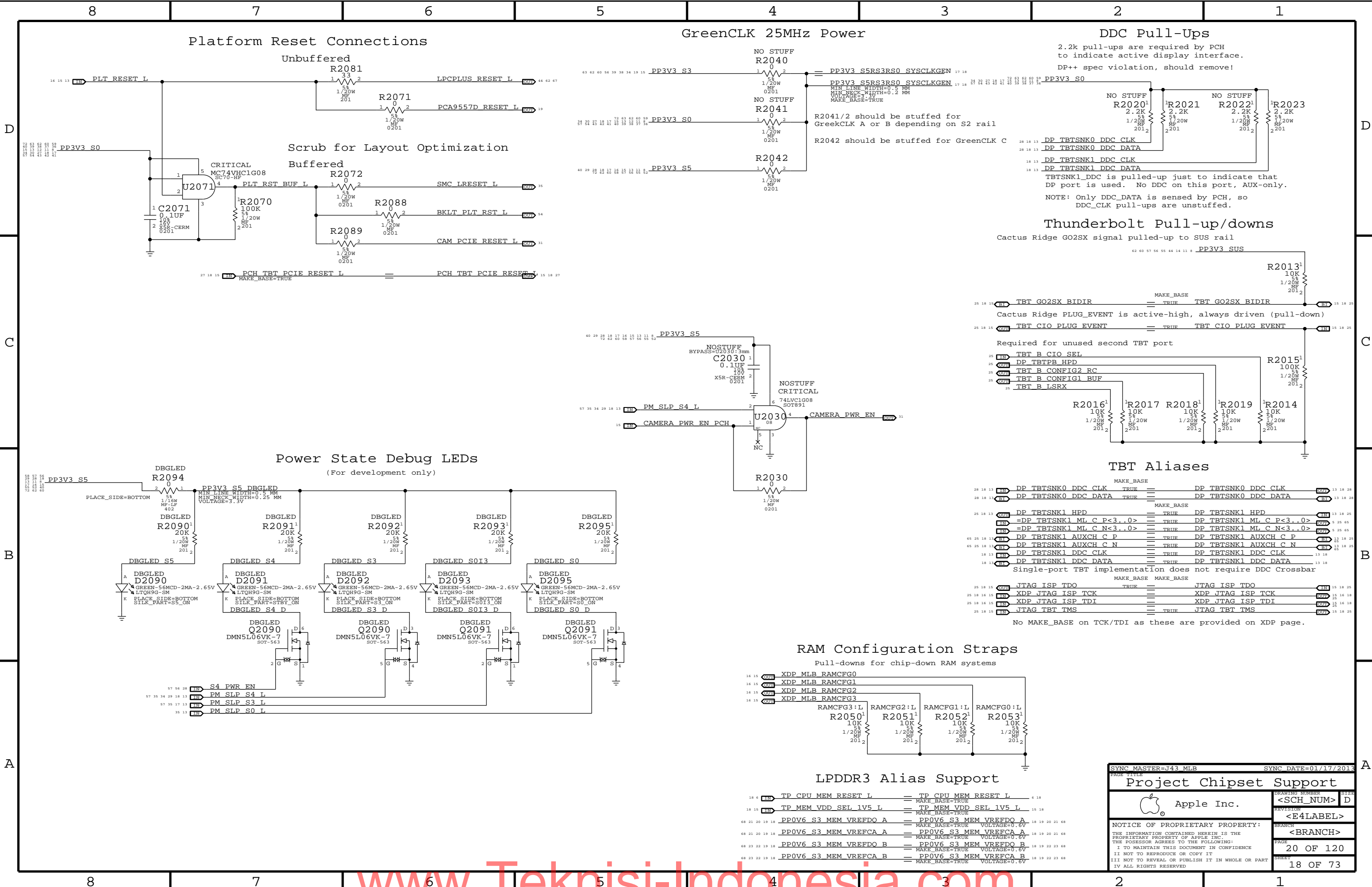
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SYNC MASTER=J43 MLB

SYNC DATE=01/17/2013

Project Chipset Support

 Apple Inc.

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Page Notes

Power aliases required by this page:

- =PP3V3_S3_VREFMRGN
- =PPDDR_S3_MEMVREF

Signal aliases required by this page:

- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:

- DDRVREF_DAC - Stuffs DAC margining circuit.

CPU-Based Margining

FETs for CPU isolation during DAC margining

NOTE: CPU DAC output step sizes:
DDR3 (1.5V) 7.70mV per step
DDR3L (1.35V) 6.99mV per step
LPDDR3 (1.2V) ???mV per step

NOTE: CPU has single output for VREFCA. Split into two signals for independent DAC margining support. When DAC margining VREFCA ensure VREFMRGN_CPU_EN is low to remove short due to CPU.

DAC-Based Margining

DAC sets voltage level, PCA9557 & FETs enable outputs and disables margining after platform reset.

OMIT

PP3V3_S3

R2218

SHORT

PP3V3_S3_VREFMRGN_DAC

MIN LINE WIDTH=0.3 mm

MIN NECK WIDTH=0.2 mm

VOLTAGE=3.3V

DDR3VREF_DAC

C2200

2.2UF

10% 6.3V XSR-CERM 402-LF

DDR3VREF_DAC

C2201

0.1UF

10% 6.3V XSR-CERM 0201

CRITICAL DDRVREF_DAC

U2200

MSOP

VDD

VOUTA

VOUTB

VOUTC

VOUTD

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VOUTF

VOUTG

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VOUTI

VOUTJ

VOUTK

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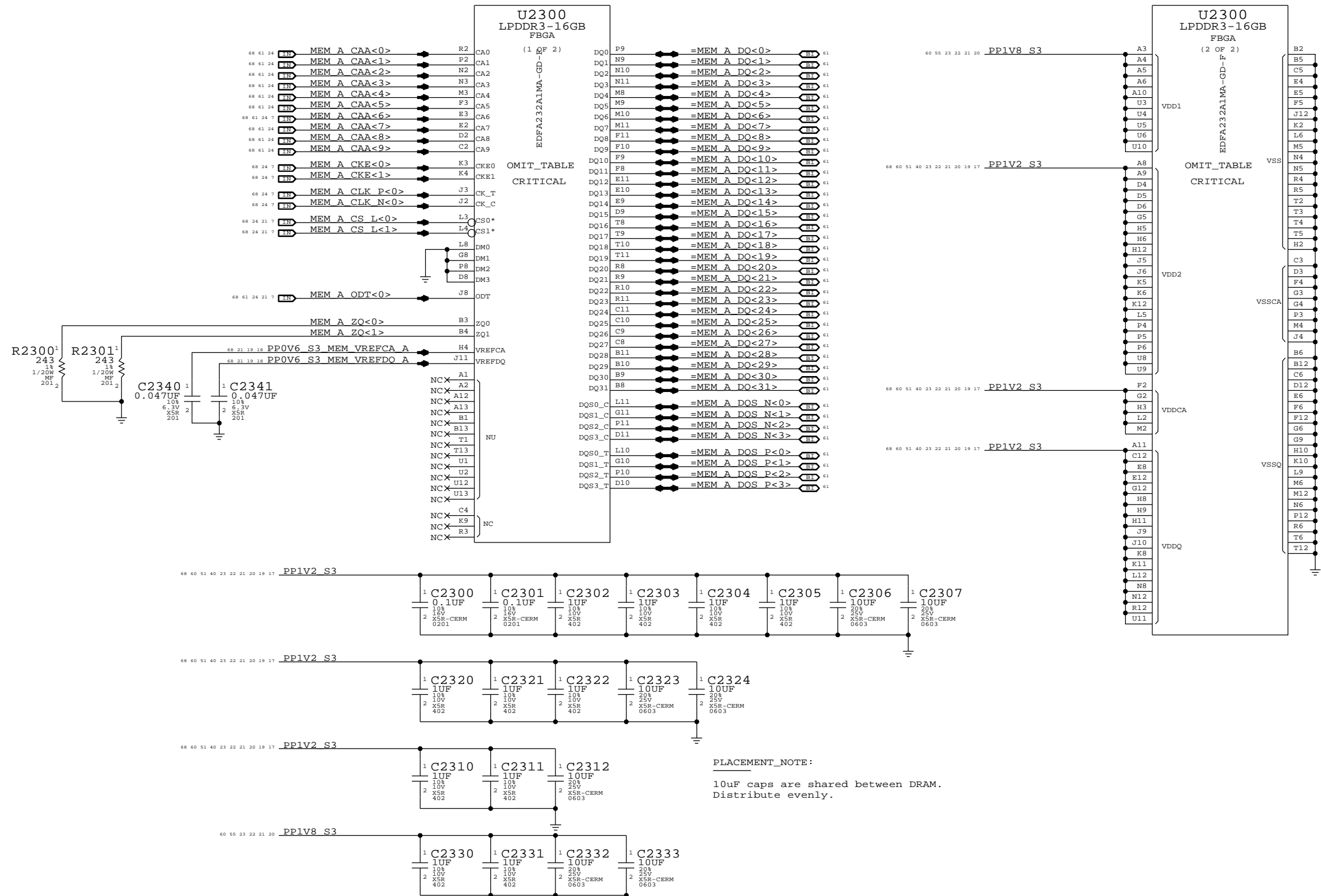
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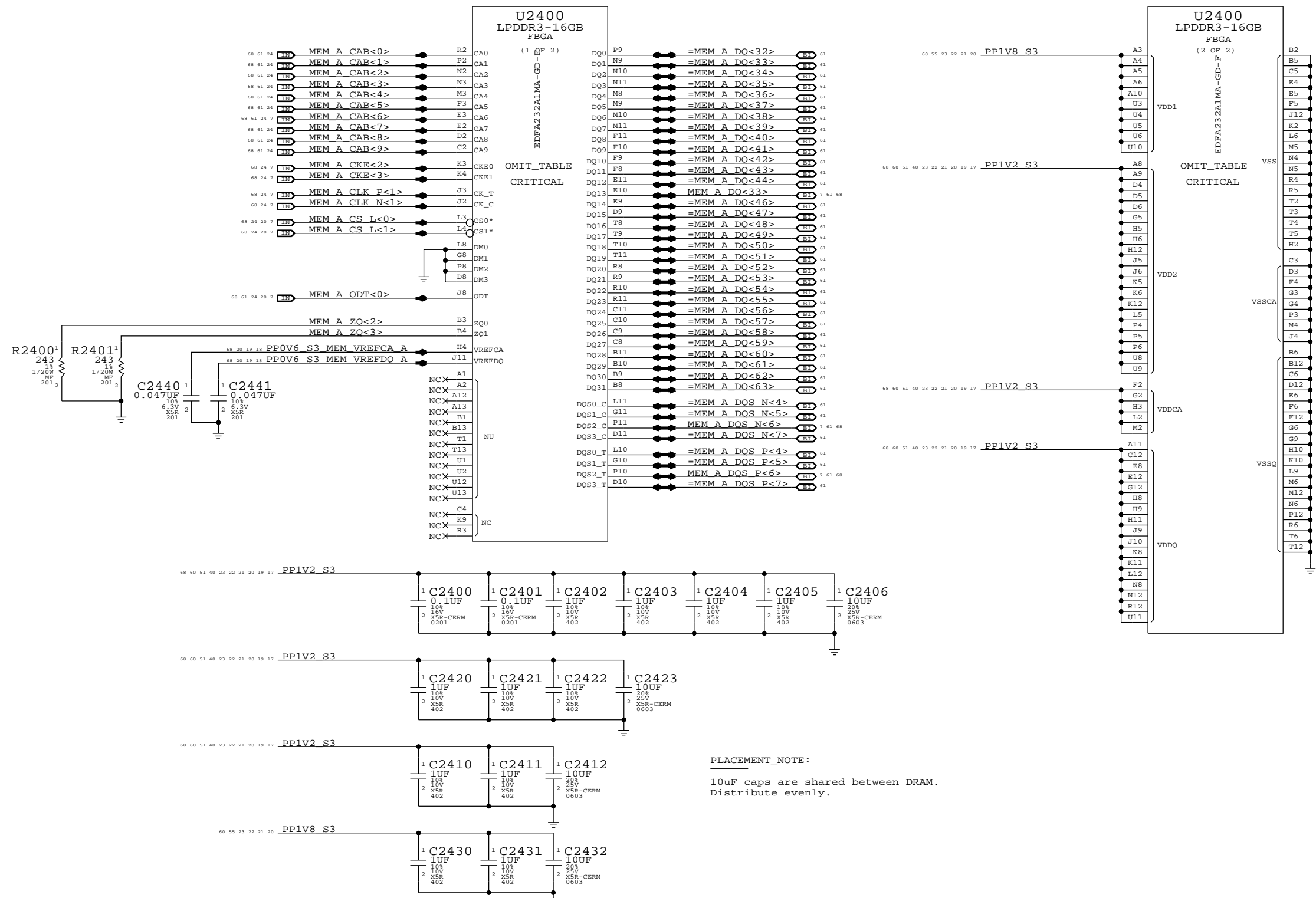
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LPDDR3 CHANNEL A (0-31)



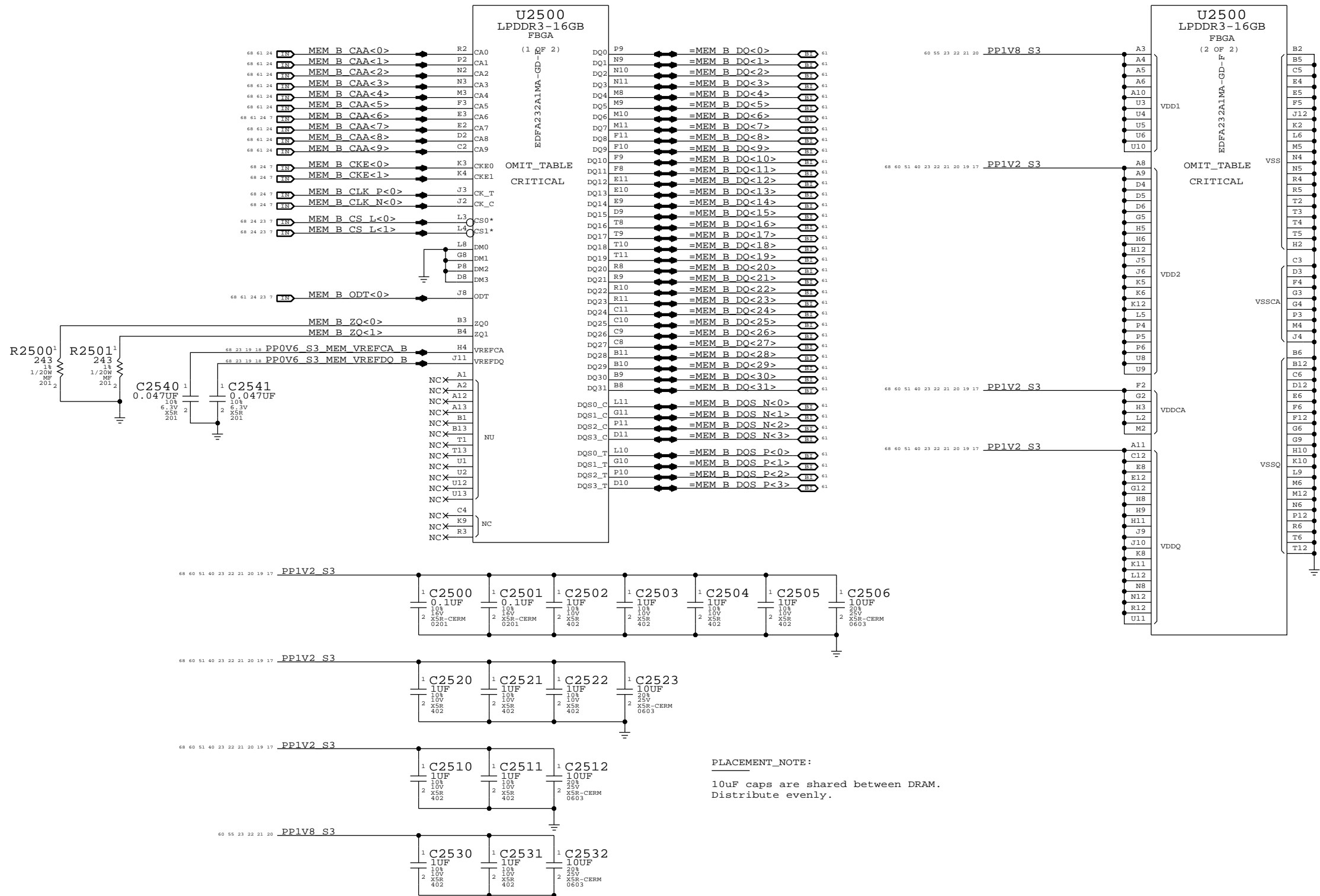
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PAGE		23 OF 120	
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LPDDR3 CHANNEL A (32-63)



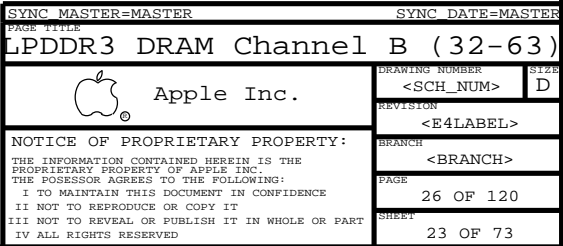
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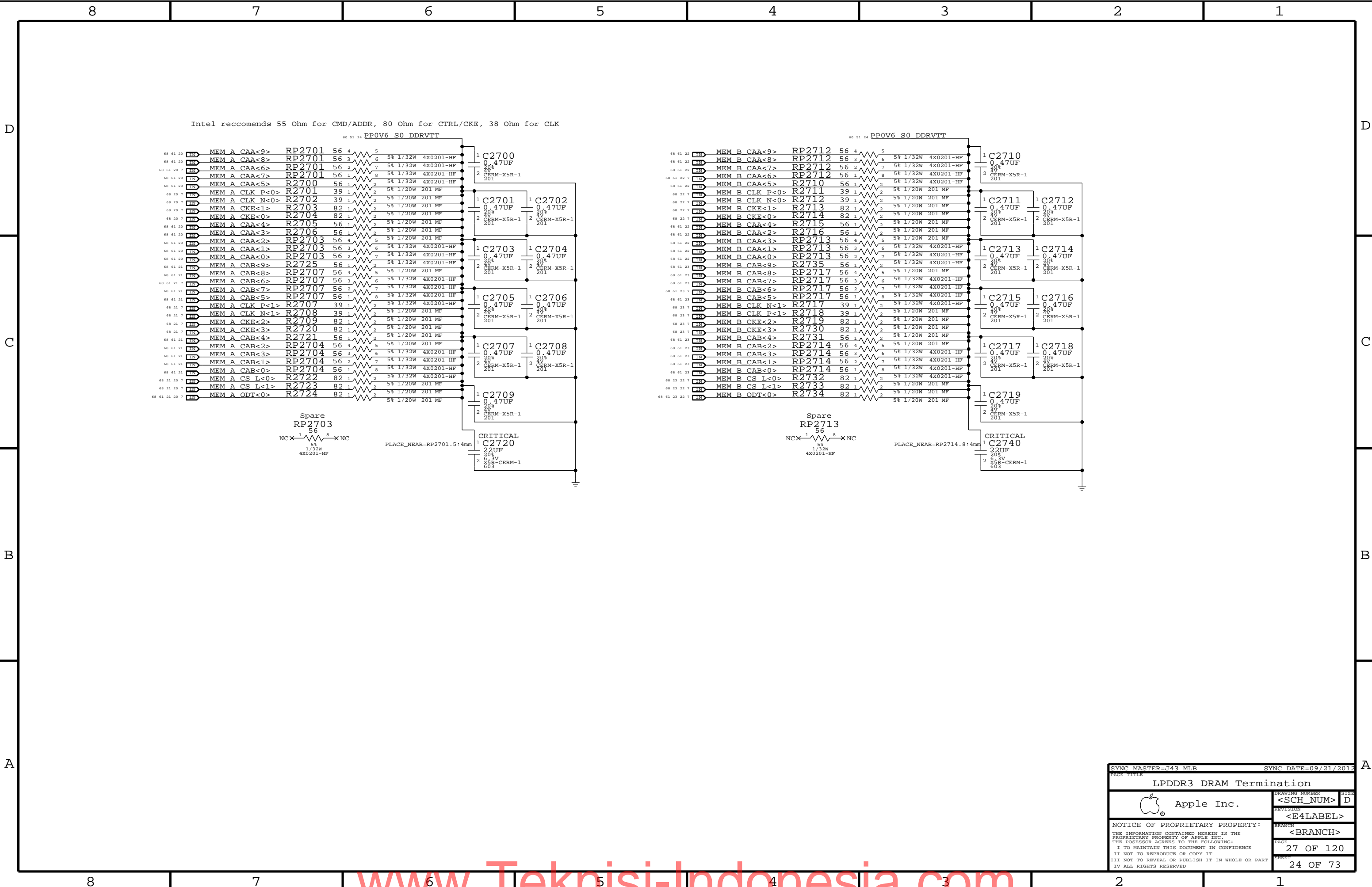
LPDDR3 CHANNEL B (0-31)

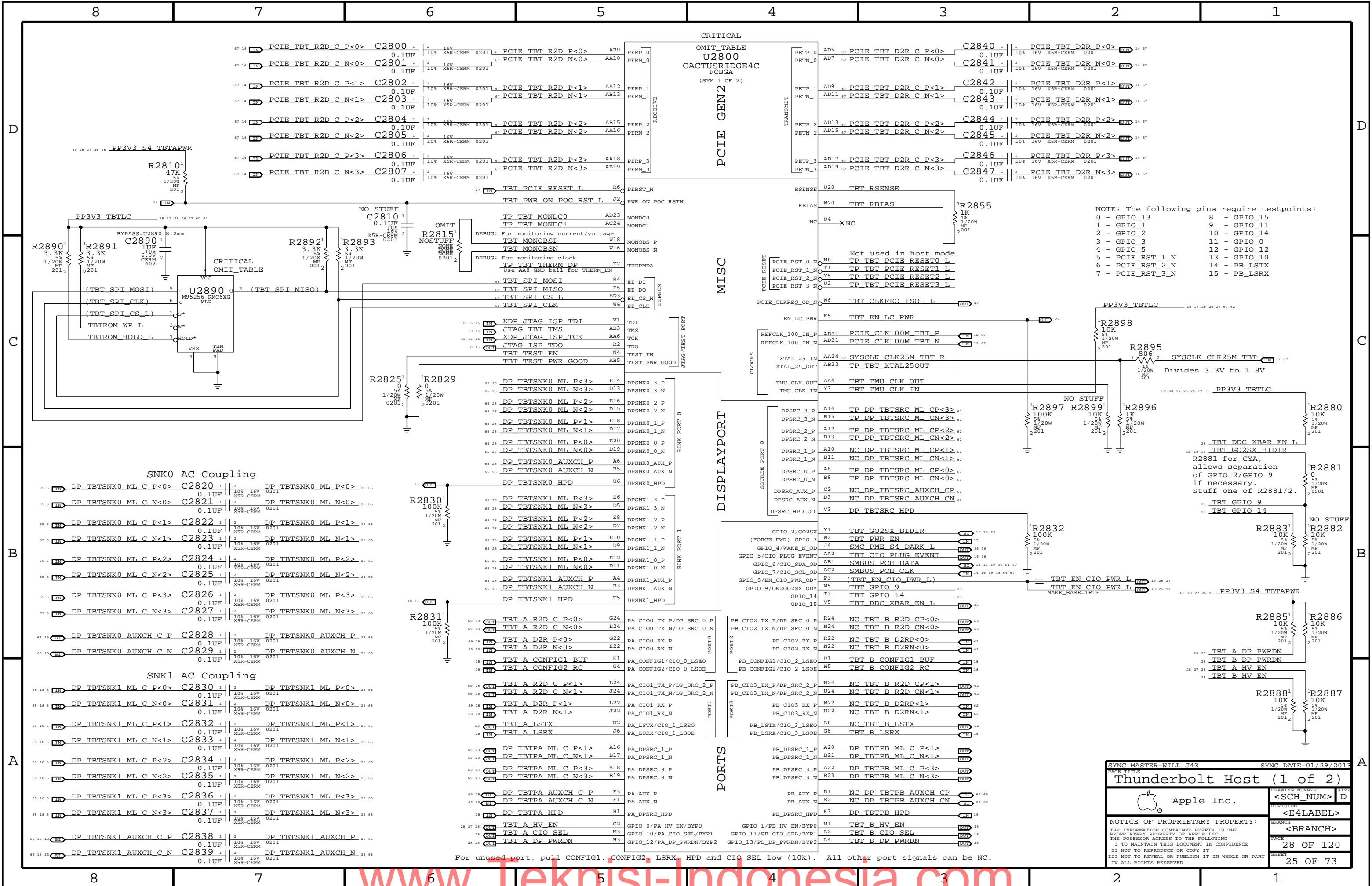


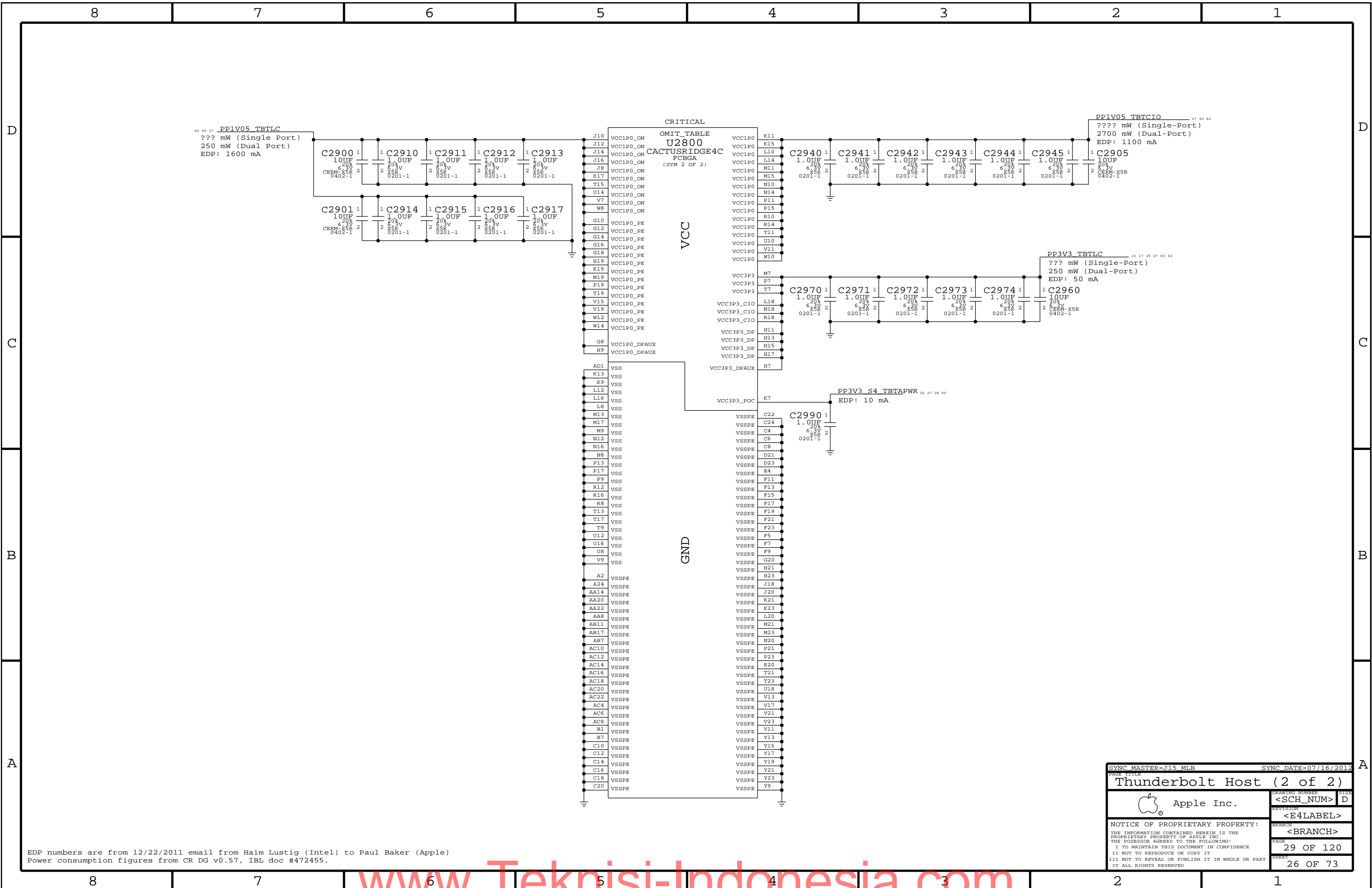
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LPDDR3 DRAM Channel B (0-31)			
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	PAGE	25 OF 120	
	SHEET	22 OF 73	

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EDP numbers are from 12/22/2011 email from Haim Lustig (Intel) to Paul Baker (Apple)
Power consumption figures from CR DG v0.57, IBL doc #472455.

SYNC MASTER=J15 MLB

SYNC DATE=07/16/2012

Thunderbolt Host (2 of 2)

 Apple Inc.

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PAGE29 OF 120

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Page Notes

Power aliases required by this page:

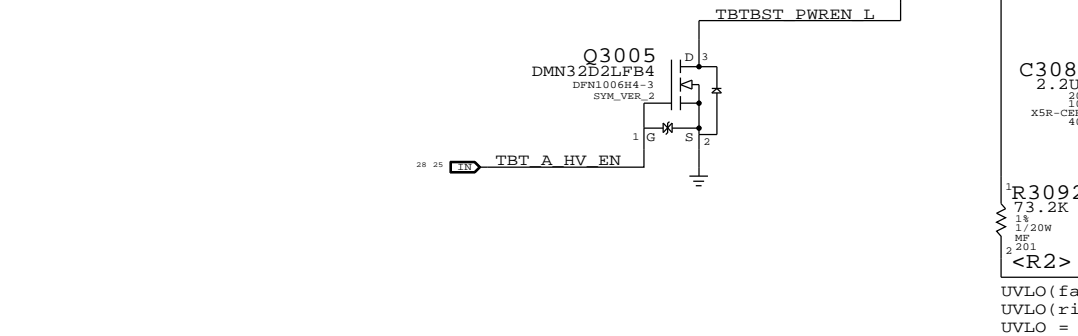
- PPVIN_SW_TBTBST (8-13V Boost Input)
- PP15V_TBT_REG (15V Boost Output)
- PP3V3_TBT_P3V3TBTFTFET (3.3V FET Input)
- PP3V3_TBT_FET (3.3V FET Output)
- PP3V3_S0_TBTTPWRCTL (8-13V Input)
- PP1V05_TBT_P1V05TBTFTFET (1.05V FET Input)
- PP1V05_TBT_FET (1.05V FET Output)

Signal aliases required by this page:

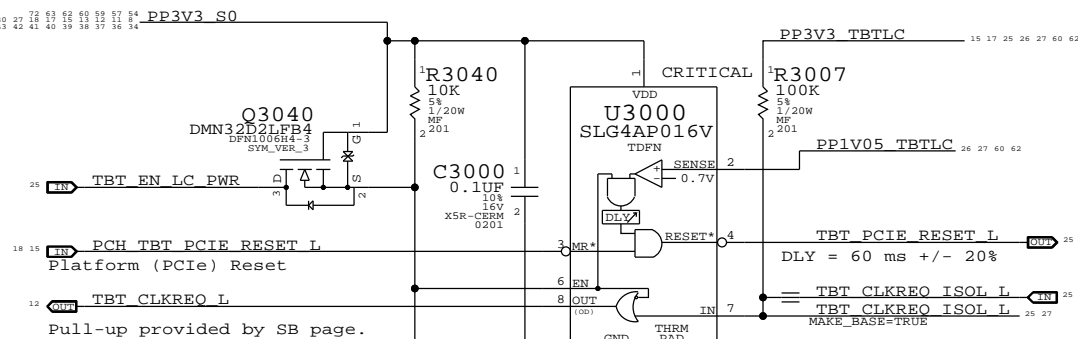
- TBT_CLKREQ_L
- TBT_RESET_L

BOM options provided by this page:

(NONE)



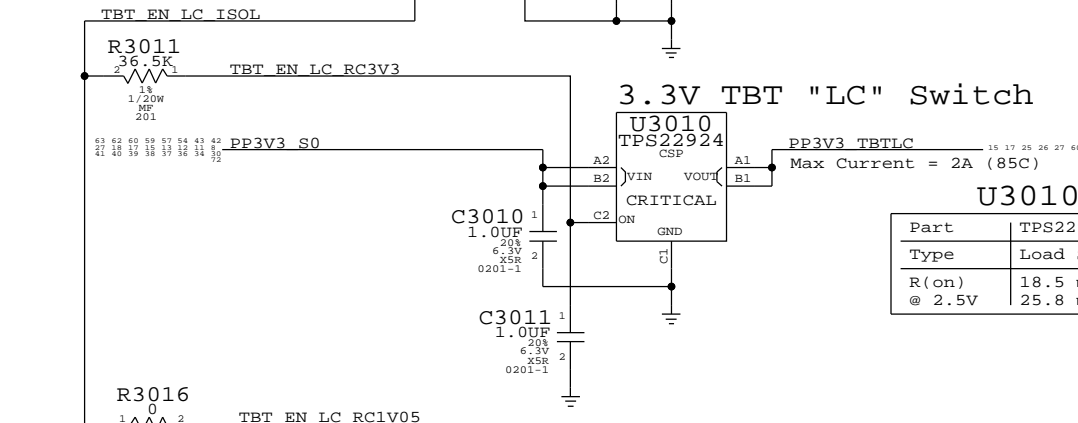
Supervisor & CLKREQ# Isolation



3.3V TBT "LC" Switch

U3010
Max Current = 2A (85C)

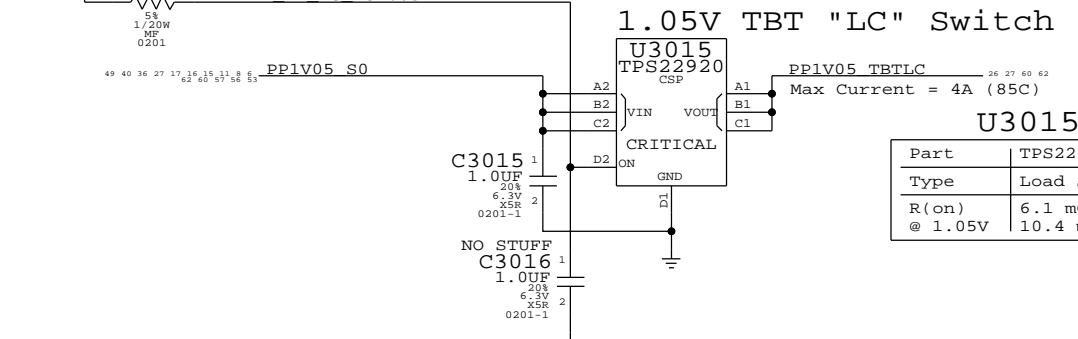
Part	TPS22924C
Type	Load Switch
R(on)	18.5 mOhm Typ
@ 2.5V	25.8 mOhm Max



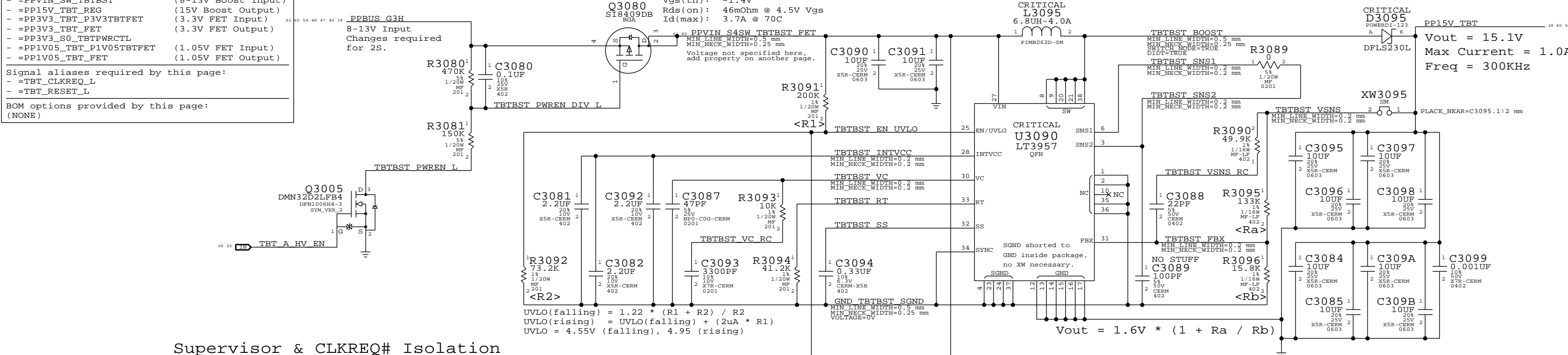
1.05V TBT "LC" Switch

U3015
Max Current = 4A (85C)

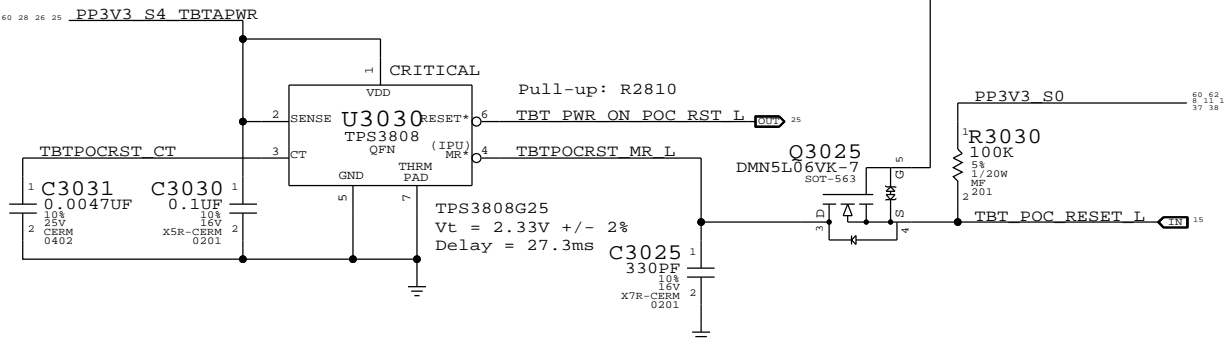
Part	TPS22920
Type	Load Switch
R(on)	6.1 mOhm Typ
@ 1.05V	10.4 mOhm Max



TBT 15V Boost Regulator



TBT "POC" Power-up Reset



1.05V TBT "CIO" Switch

U3020
Max Current = 4A (85C)

Part	TPS22920
Type	Load Switch
R(on)	6.1 mOhm Typ
@ 1.05V	10.4 mOhm Max

SYNC MASTER=WILL J43

SYNC DATE=12/17/2012

TBT Power Support

Apple Inc.

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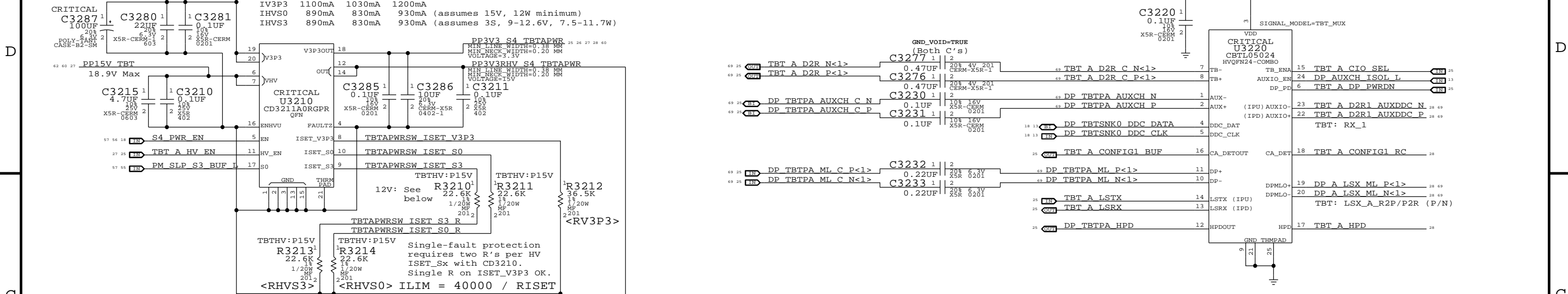
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SHEET

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8	7	6	5	4	3	2	1
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	Nominal	Min	Max
PP3V3_S5			
PP3V3_S4_1BIAPWR			

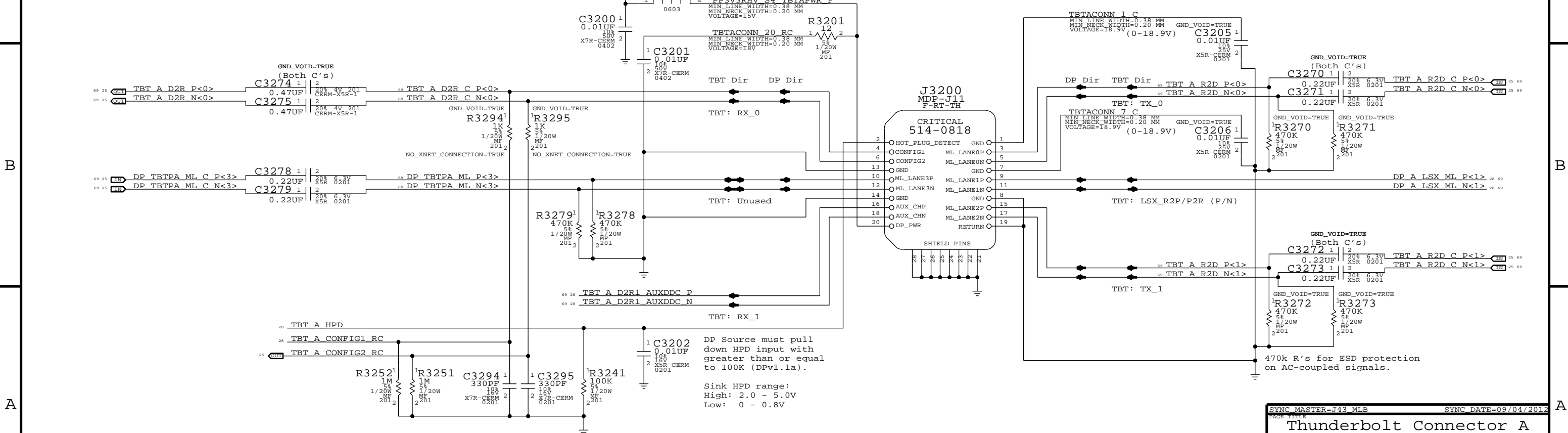


For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3210,R3213		TBTHV:P12V
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3211,R3214		TBTHV:P12V

	Nominal	Min	Max	
IHVS0/S3	1120mA	1090mA	1170mA	(12W minimum)

IHVS0/S3 1120mA 1090mA 1170mA (12W minimum)



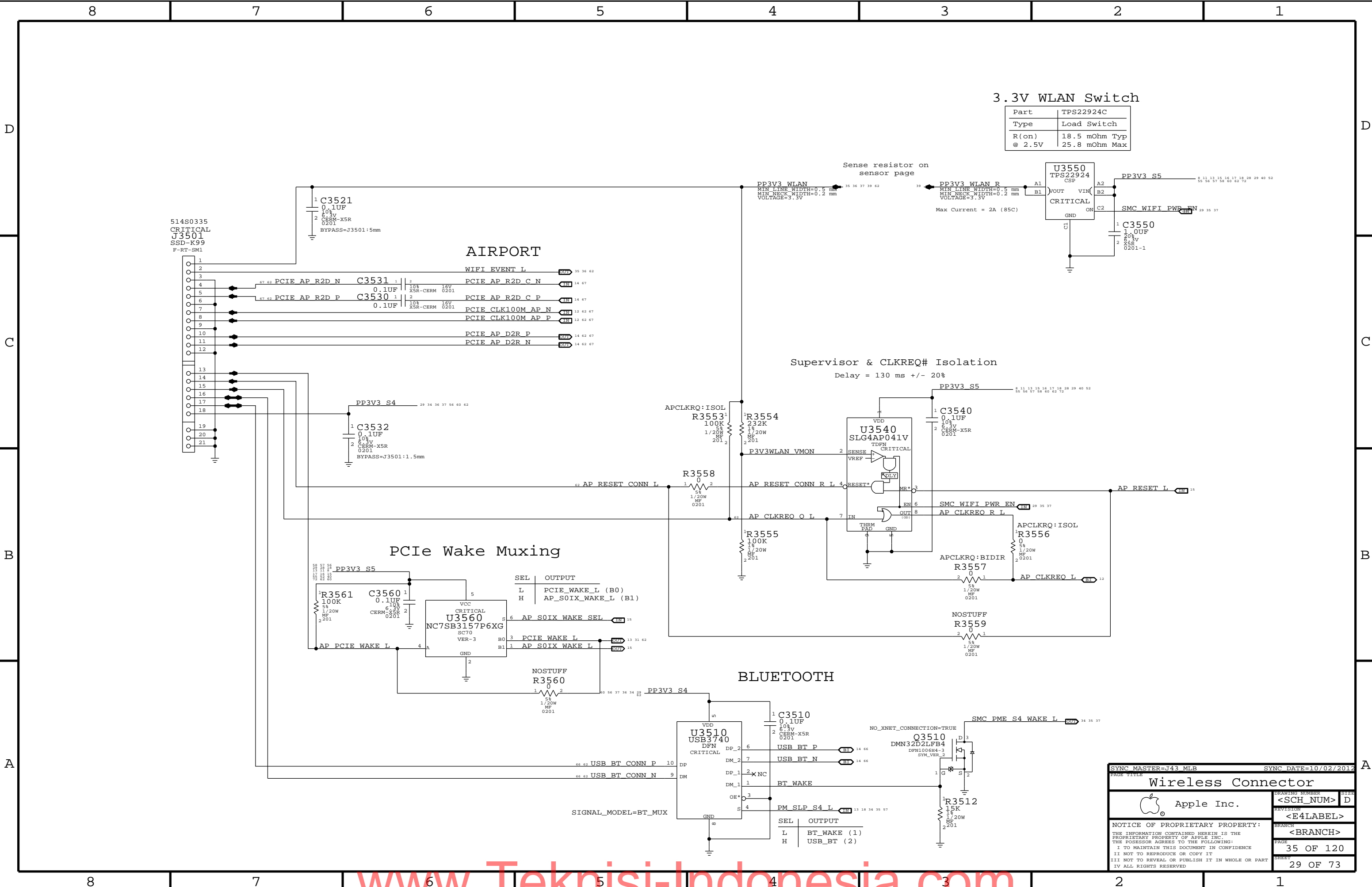
DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).

[illegible]

A

Low: 0 - 0.8V

SYNC MASTER=J43 MLB		SYNC DATE=09/04/2012	
PAGE TITLE			
Thunderbolt Connector A		DRAWING NUMBER	SIZE
Apple Inc.		<SCH_NUM>	D
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		PAGE	32 OF 120
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3.3V WLAN Switch

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max

Supervisor & CLKREQ# Isolation
Delay = 130 ms +/- 20%

PCIe Wake Muxing

BLUETOOTH

SYNC MASTER=J43 MLB		SYNC DATE=10/02/2012	
PAGE TITLE			
Wireless Connector			
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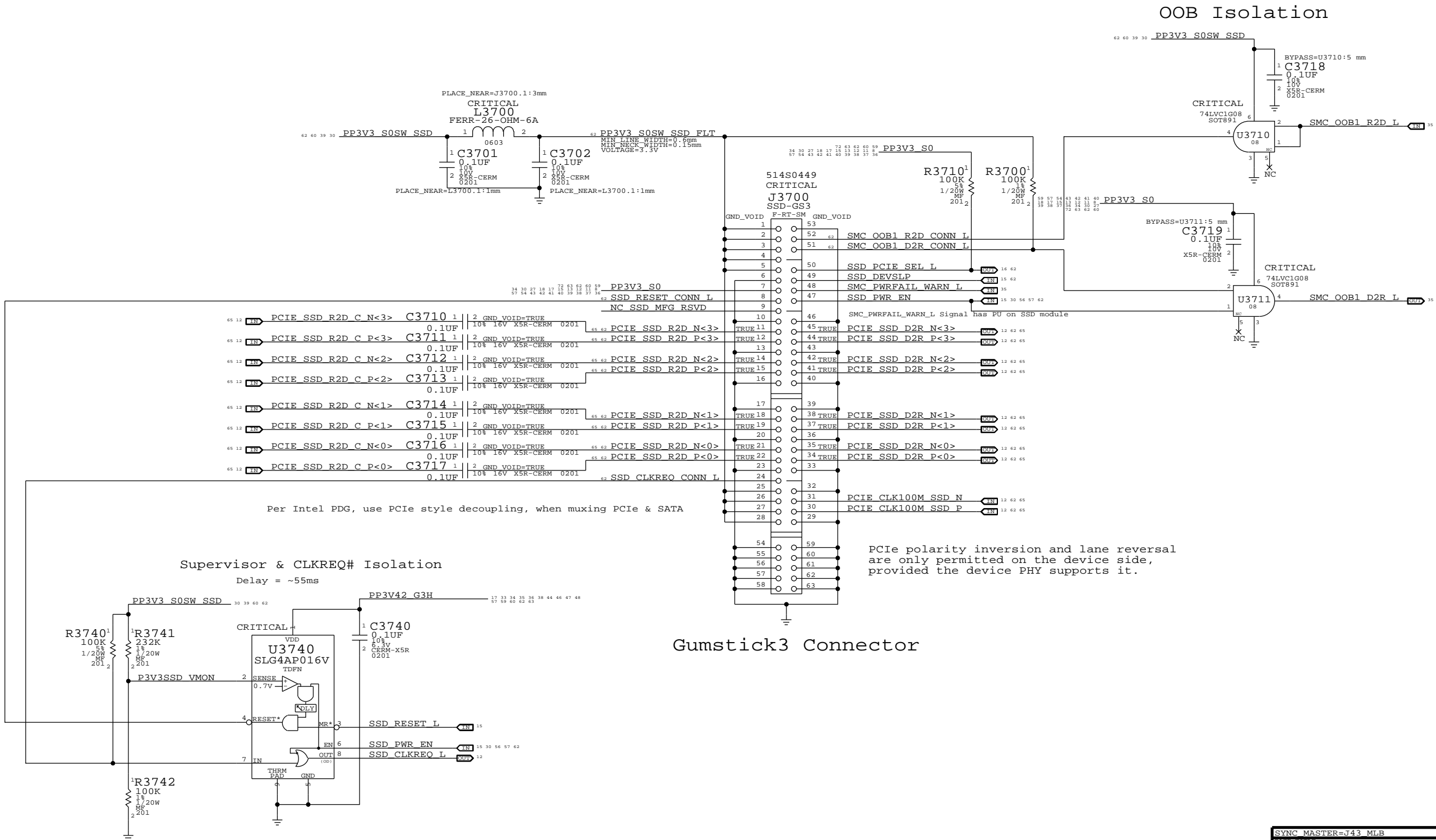
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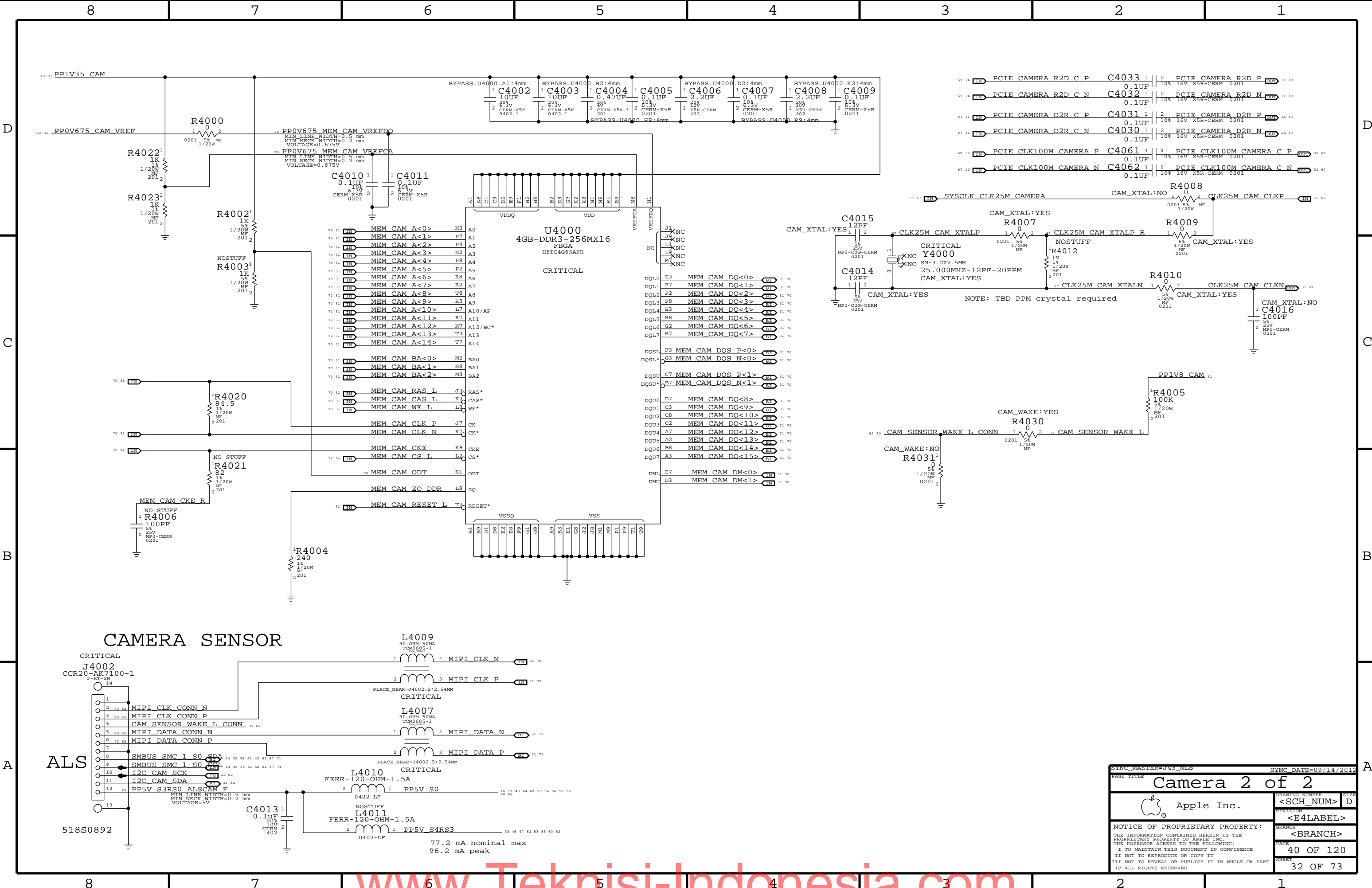
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SYNC MASTER=J43 MLB		SYNC DATE=02/20/2013	
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SSD Connector			
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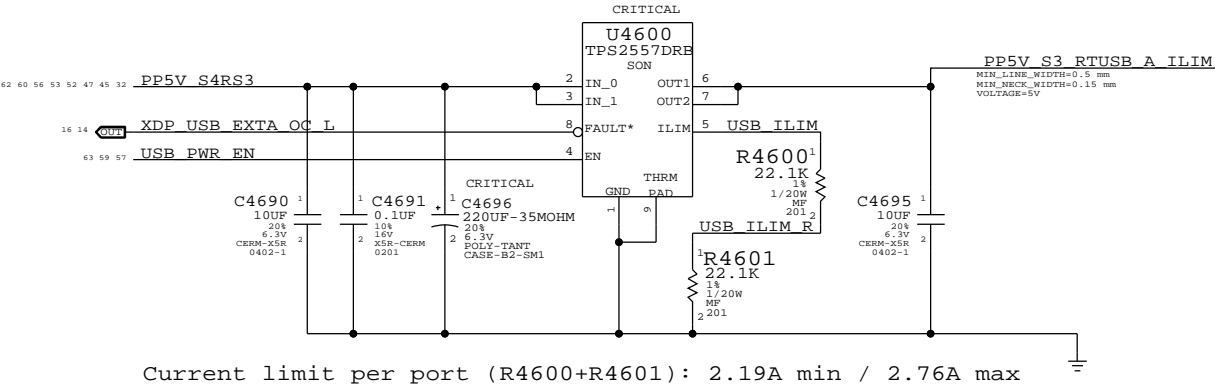




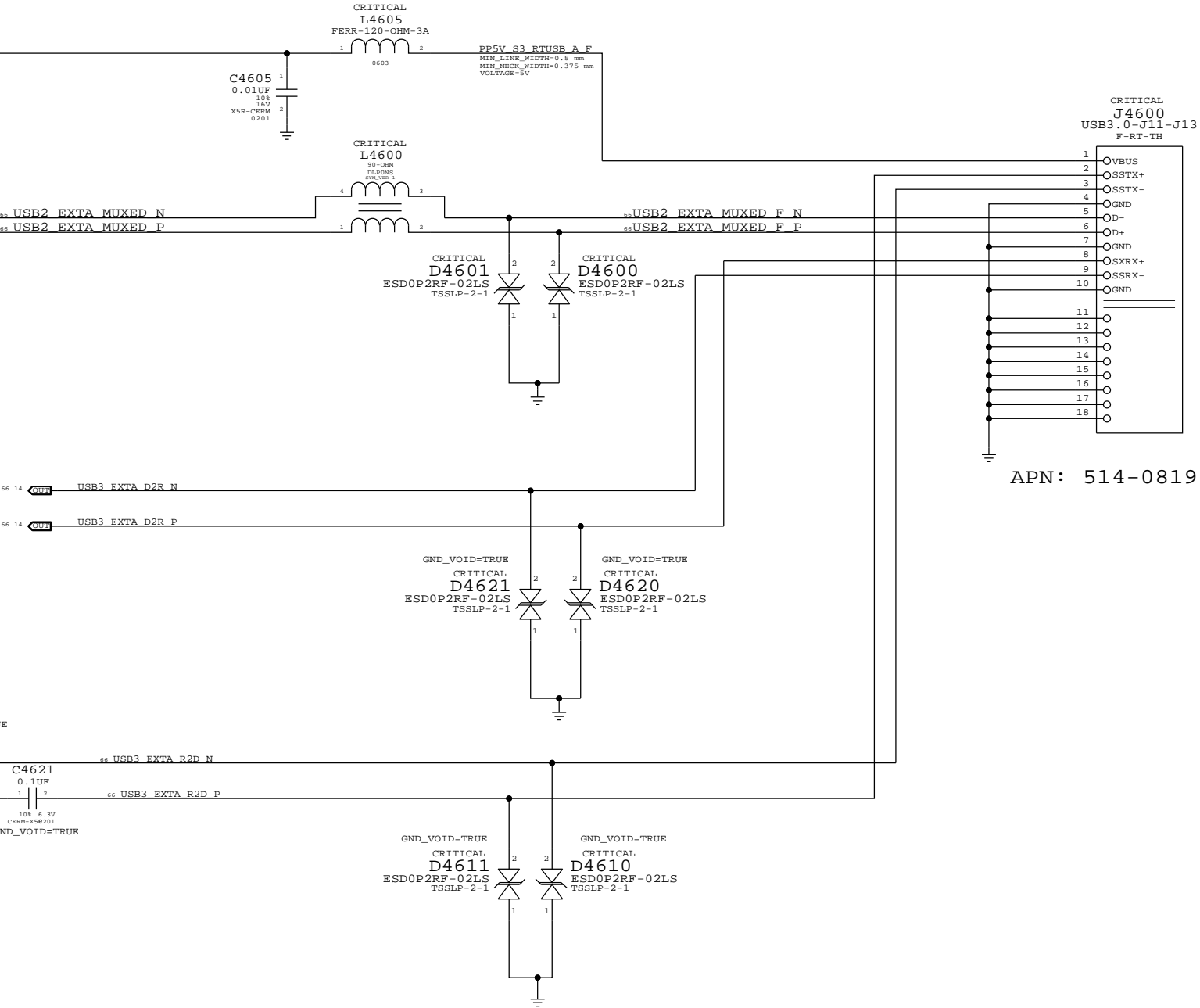
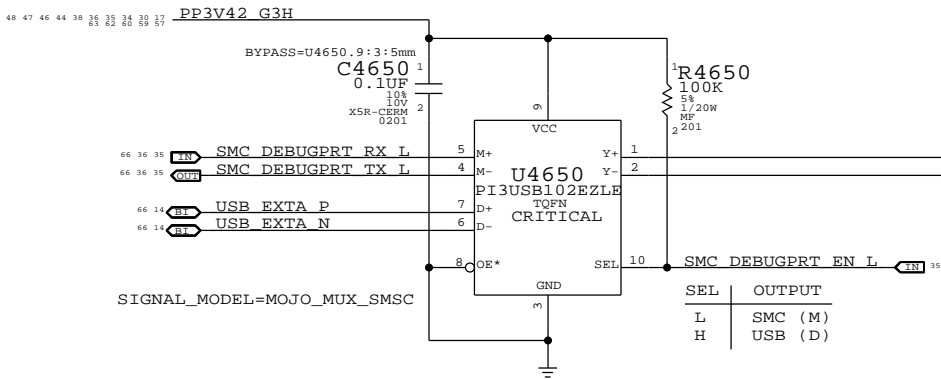
Camera 2 of 2		Apple Inc.	
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		PAGE	
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Right USB Port A

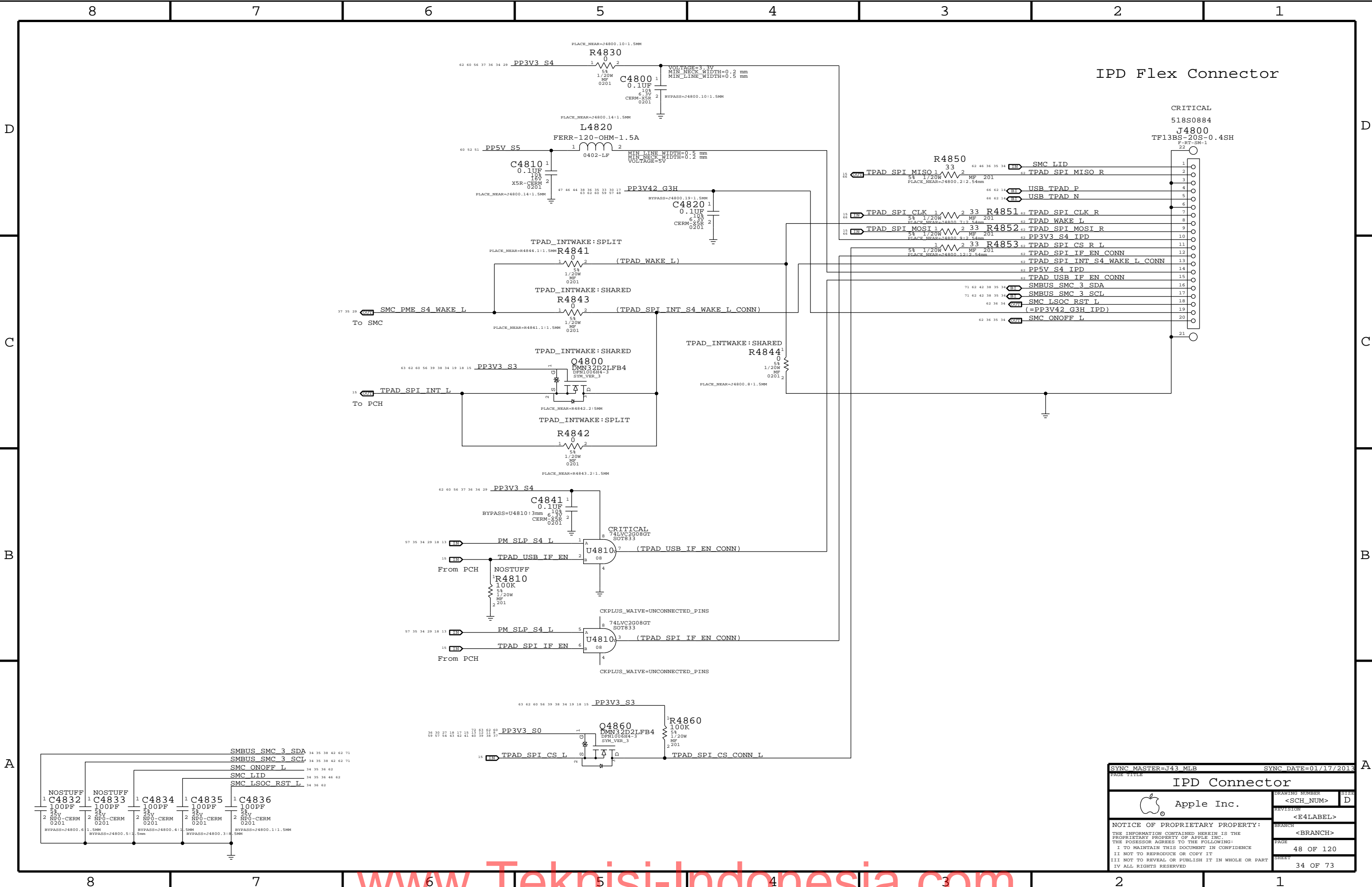
USB Port Power Switch



Mojo SMC Debug Mux



SYNC MASTER=J43 MLB		SYNC DATE=02/20/2013	
PAGE TITLE			
External A USB3 Connector			
 Apple Inc.	DRAWING NUMBER	SIZE	
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IPD Flex Connector

CRITICAL

518S0884

J4800

TF13BS-20S-0.4SH

F-RT-SM-1

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
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PAGE TITLE		PAGE NUMBER	
IPD Connector		48 OF 120	
Apple Inc.		34 OF 73	
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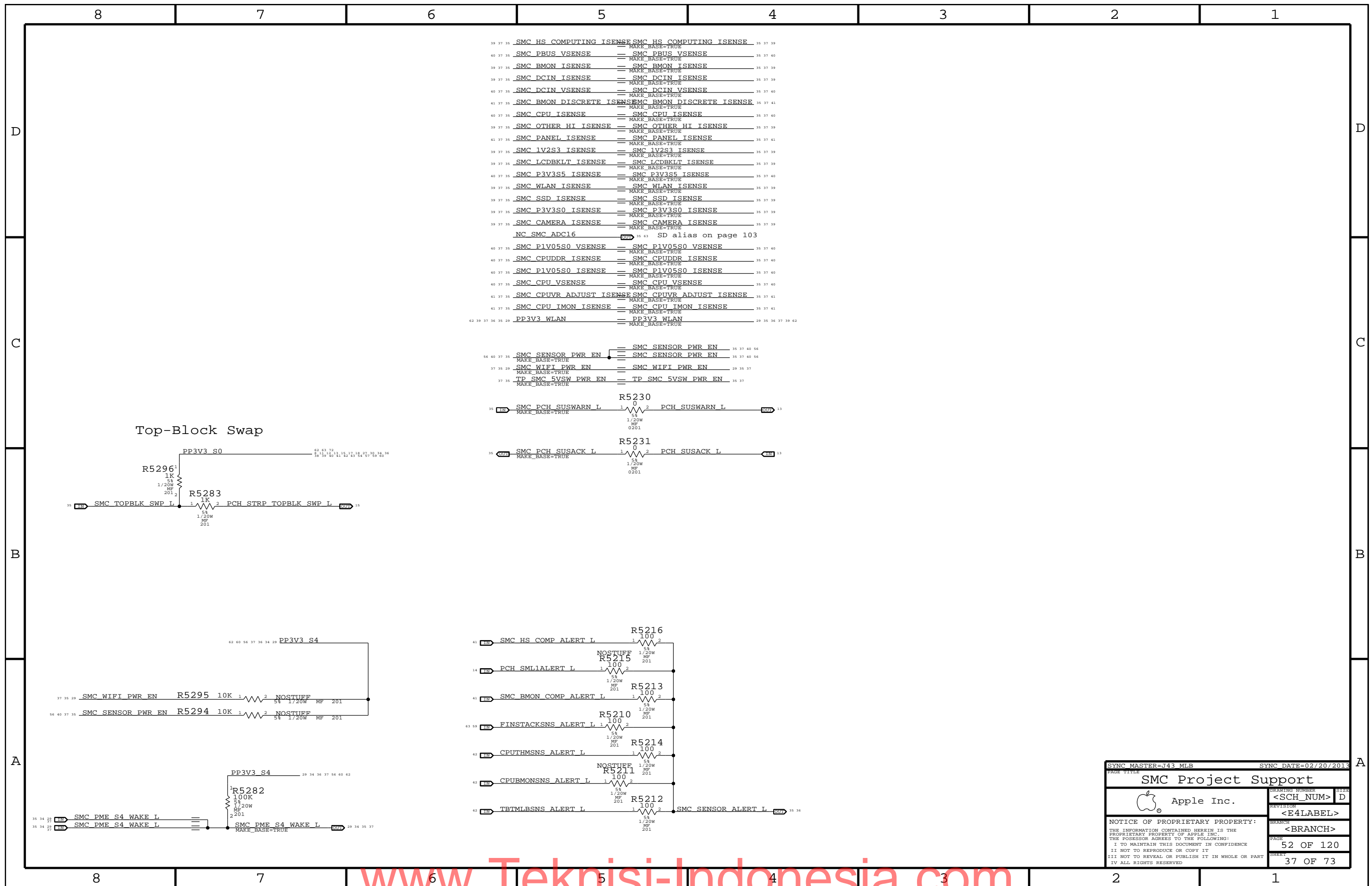


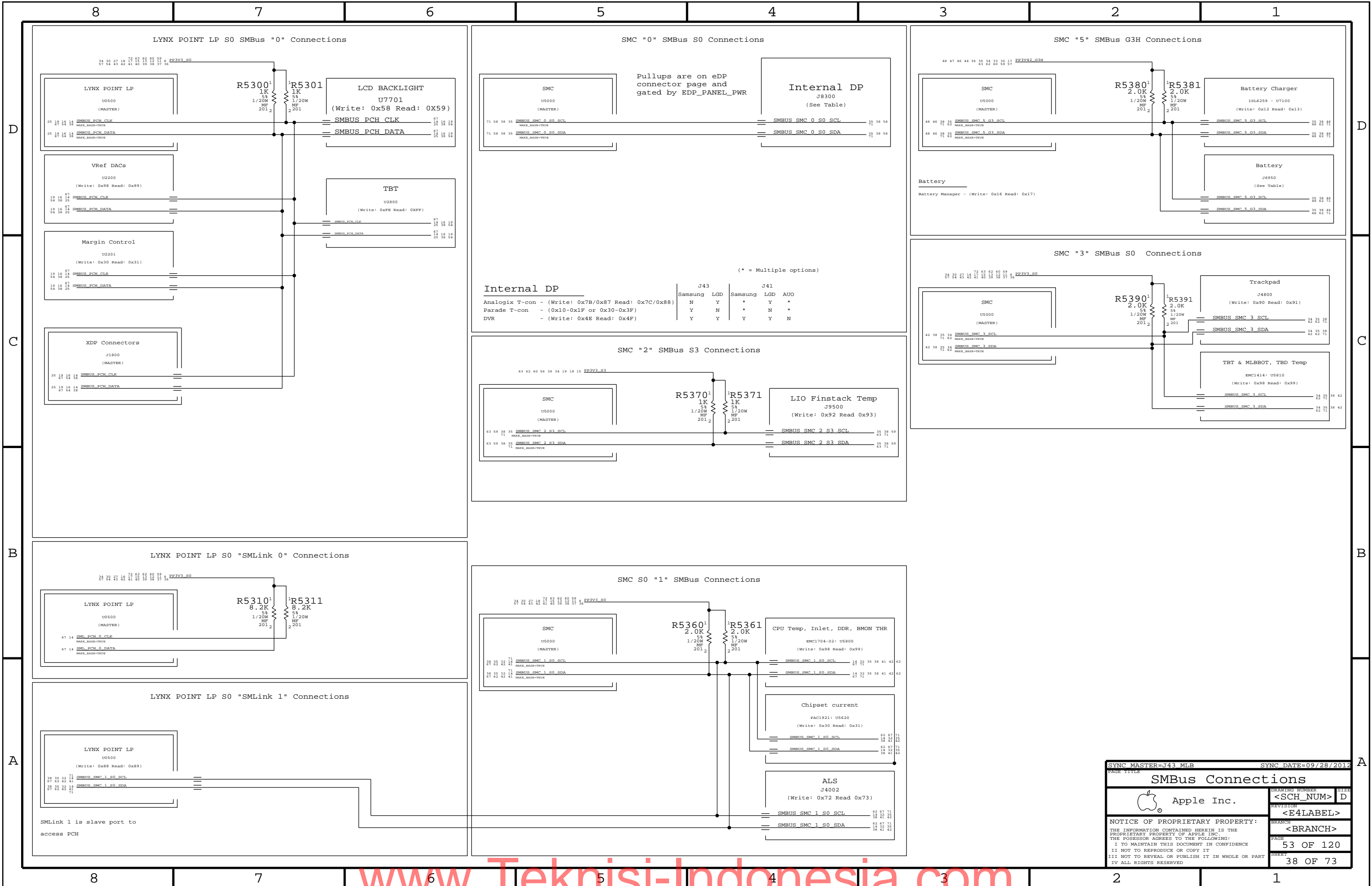
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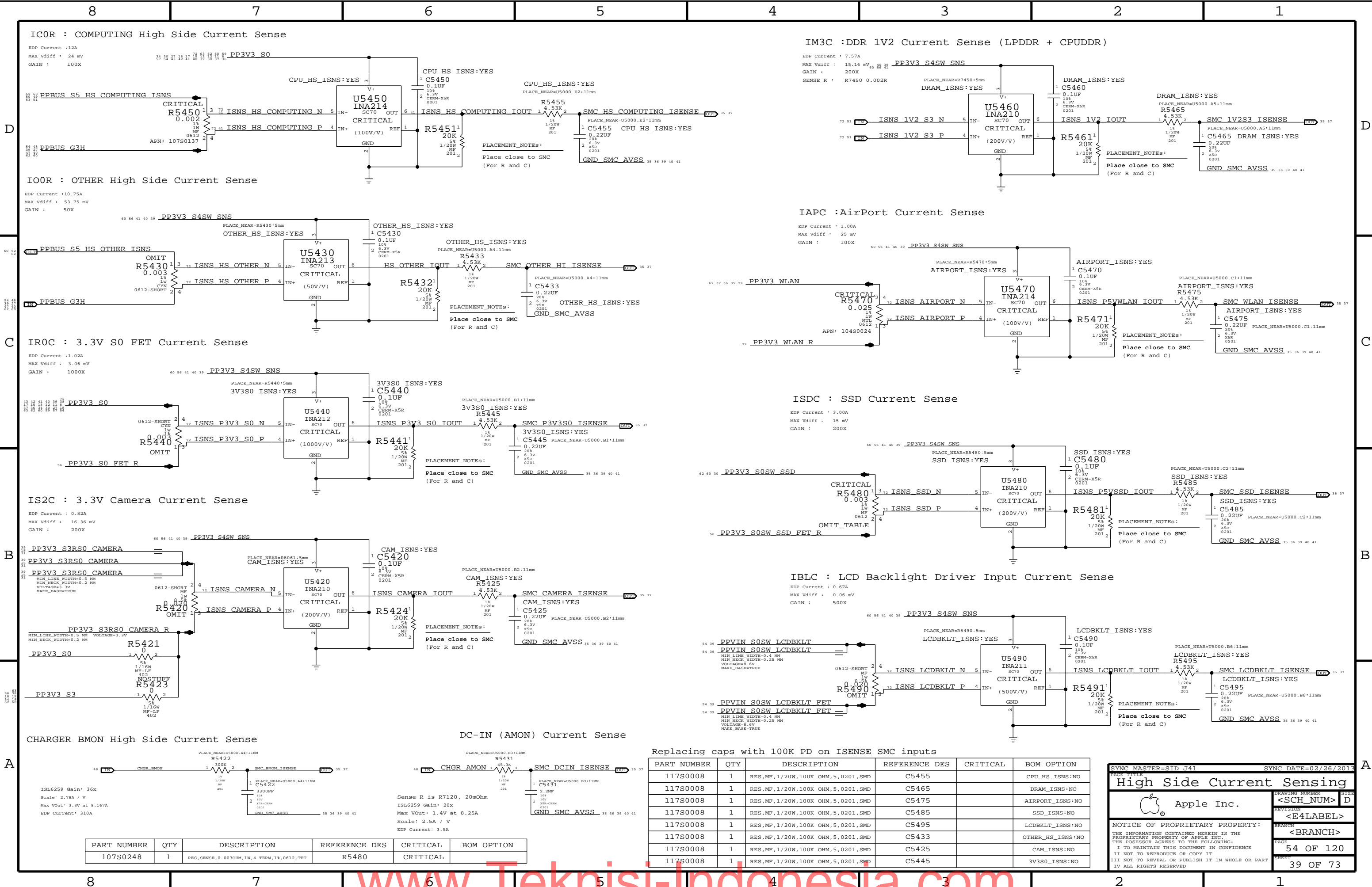
B





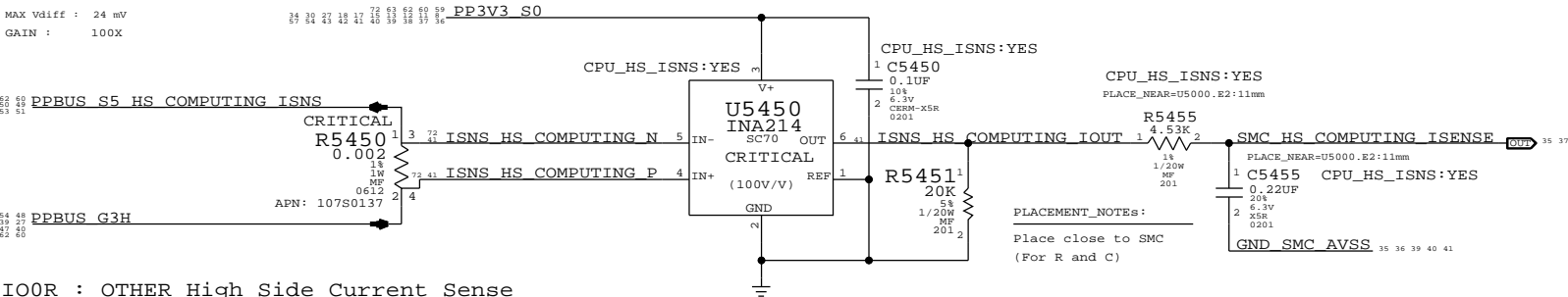






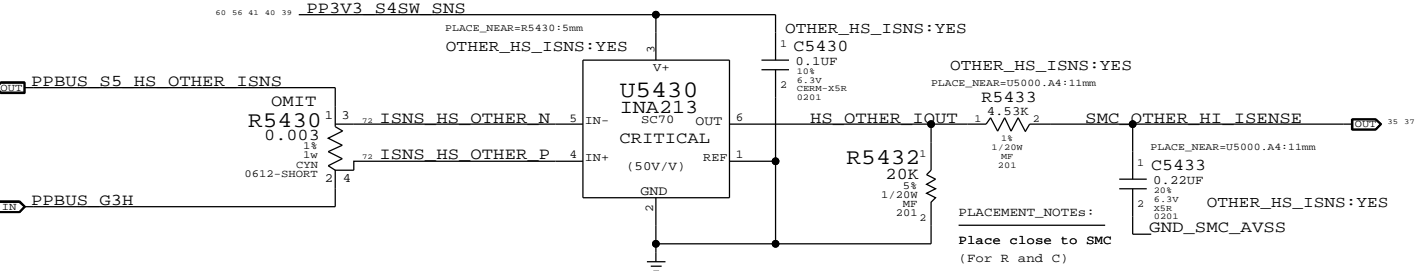
IC0R : COMPUTING High Side Current Sense

EDP Current : 12A
MAX Vdiff : 24 mV
GAIN : 100X



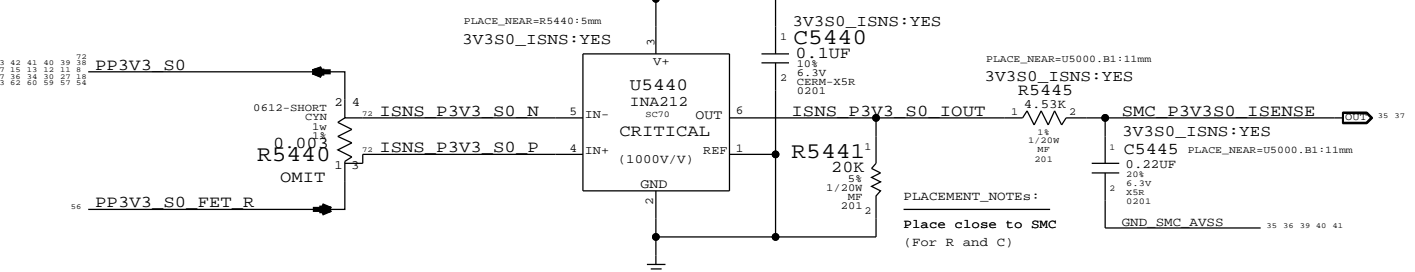
IO0R : OTHER High Side Current Sense

EDP Current : 10.75A
MAX Vdiff : 53.75 mV
GAIN : 50X



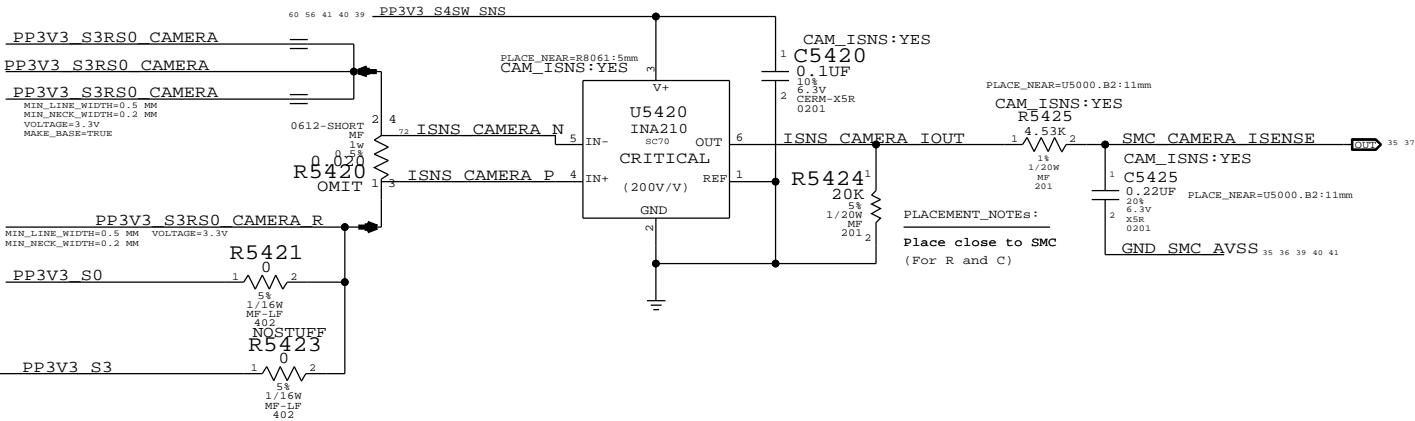
IR0C : 3.3V S0 FET Current Sense

EDP Current : 1.02A
MAX Vdiff : 3.06 mV
GAIN : 1000X

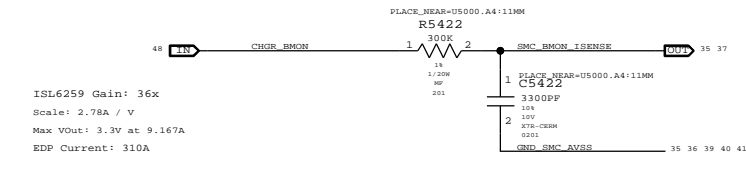


IS2C : 3.3V Camera Current Sense

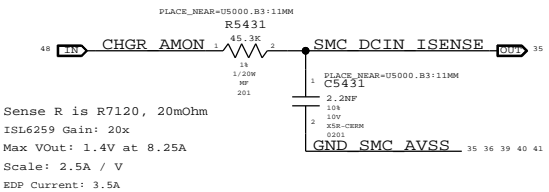
EDP Current : 0.82A
MAX Vdiff : 16.36 mV
GAIN : 200X



CHARGER BMON High Side Current Sense



DC-IN (AMON) Current Sense

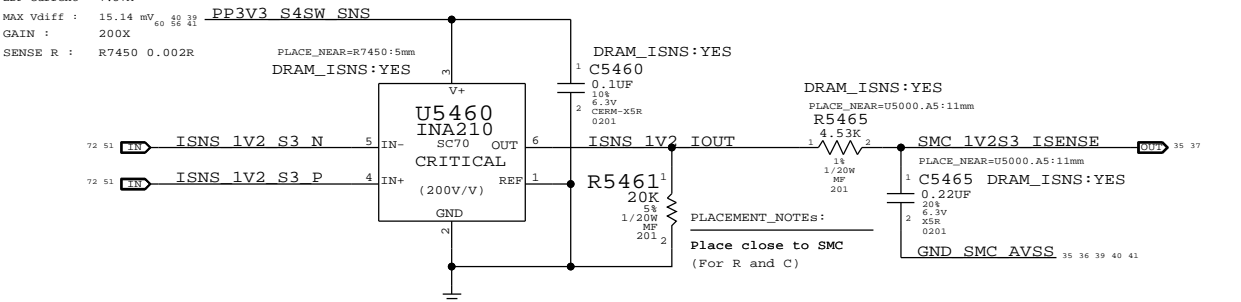


Replacing caps with 100K PD on ISENSE SMC inputs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5455		CPU_HS_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5465		DRAM_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5475		AIRPORT_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5495		SSD_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5433		OTHER_HS_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5425		CAM_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5445		3V3S0_ISNS:NO

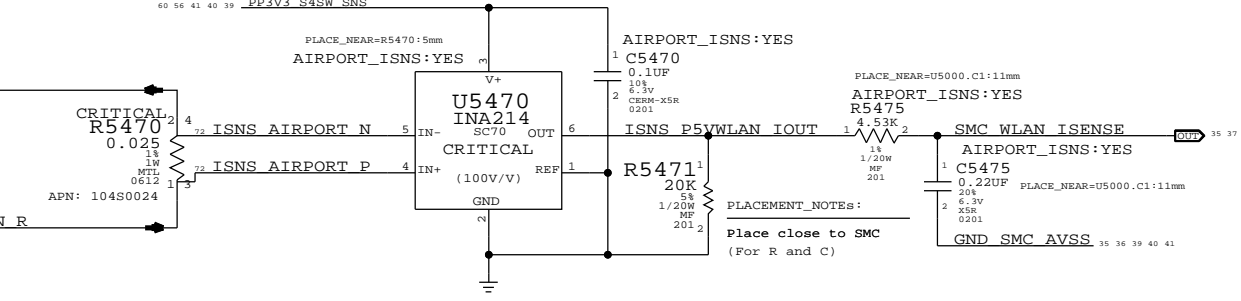
IM3C :DDR 1V2 Current Sense (LPDDR + CPUDDR)

EDP Current : 7.57A
MAX Vdiff : 15.14 mV
GAIN : 200X
SENSE R : R7450 0.002R



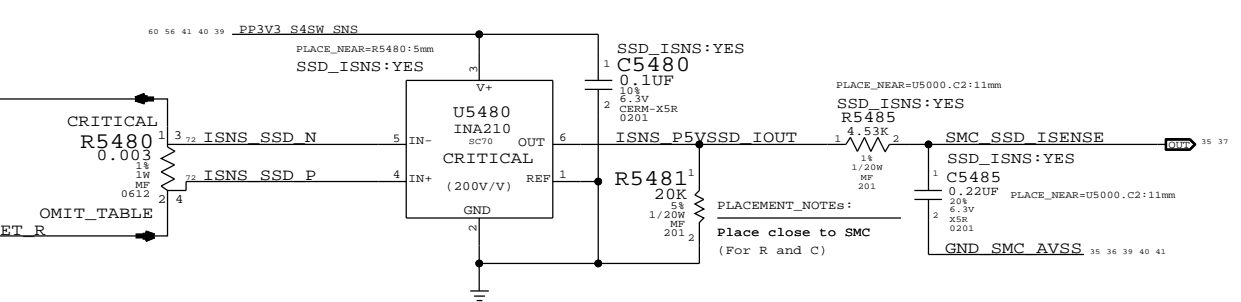
IAPC :AirPort Current Sense

EDP Current : 1.00A
MAX Vdiff : 25 mV
GAIN : 100X



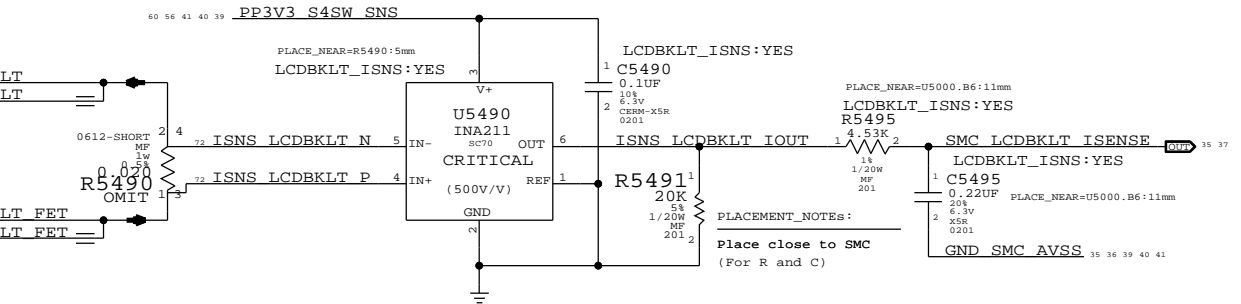
ISDC : SSD Current Sense

EDP Current : 3.00A
MAX Vdiff : 15 mV
GAIN : 200X



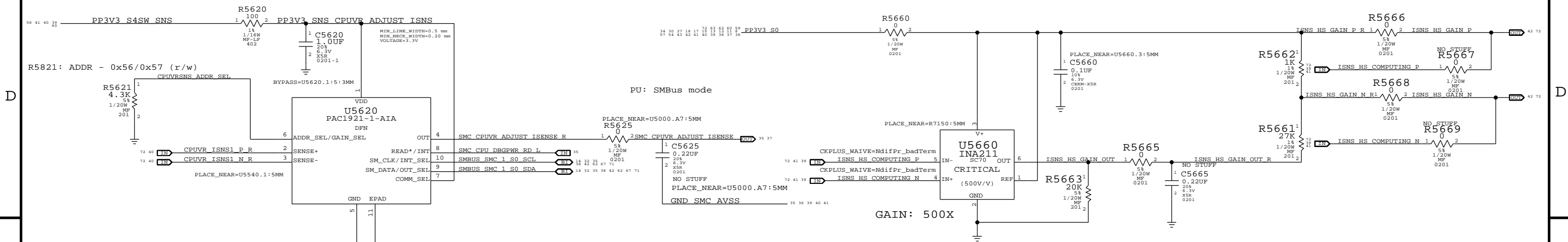
IBLC : LCD Backlight Driver Input Current Sense

EDP Current : 0.67A
MAX Vdiff : 0.06 mV
GAIN : 500X



ICS3 : Adjustable Gain CPU VR Current

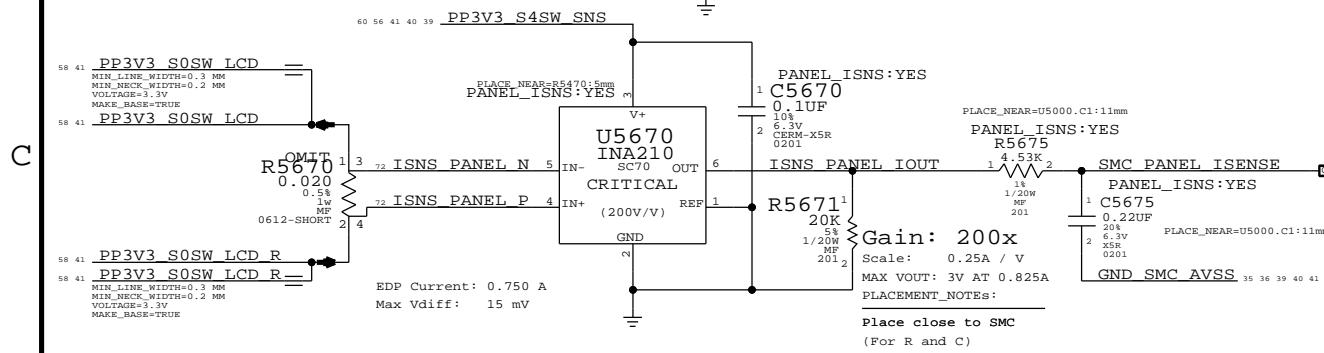
Sense Pins gain stage for U5800 (EMC1704)



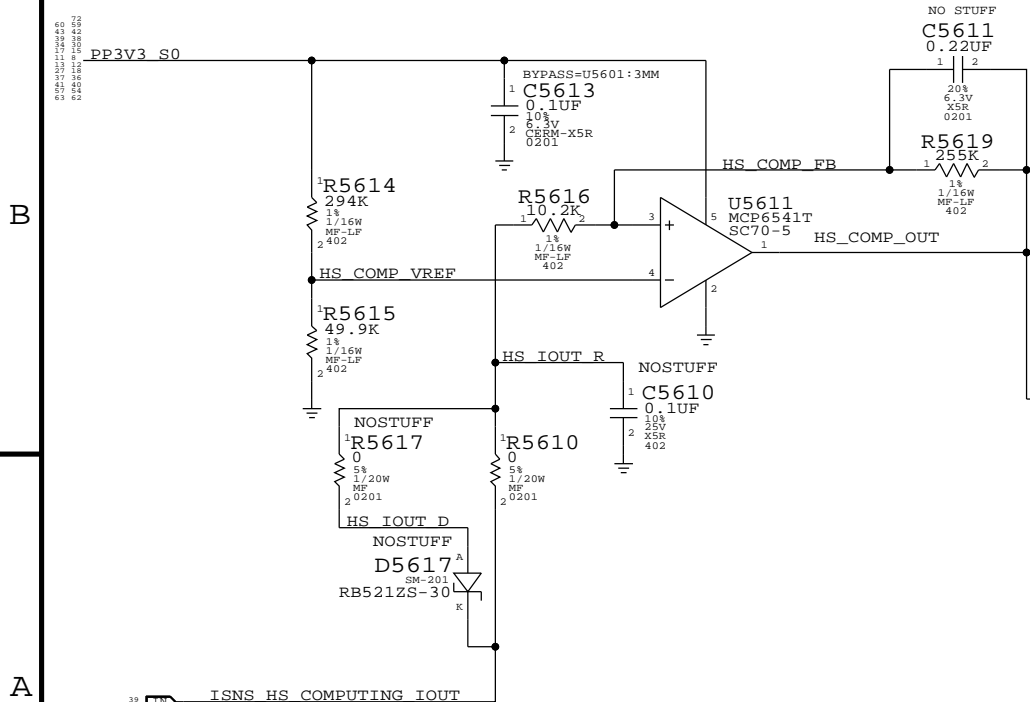
In battery discharge scenario negative voltage will be present on IN+/- pins with INA output voltage decreasing from 3.3V with increasing discharge current.

With 100mA battery current, Will have 10.2mV difference going into sense pins of U5800. This will set the minimum current threshold at 0.100mA

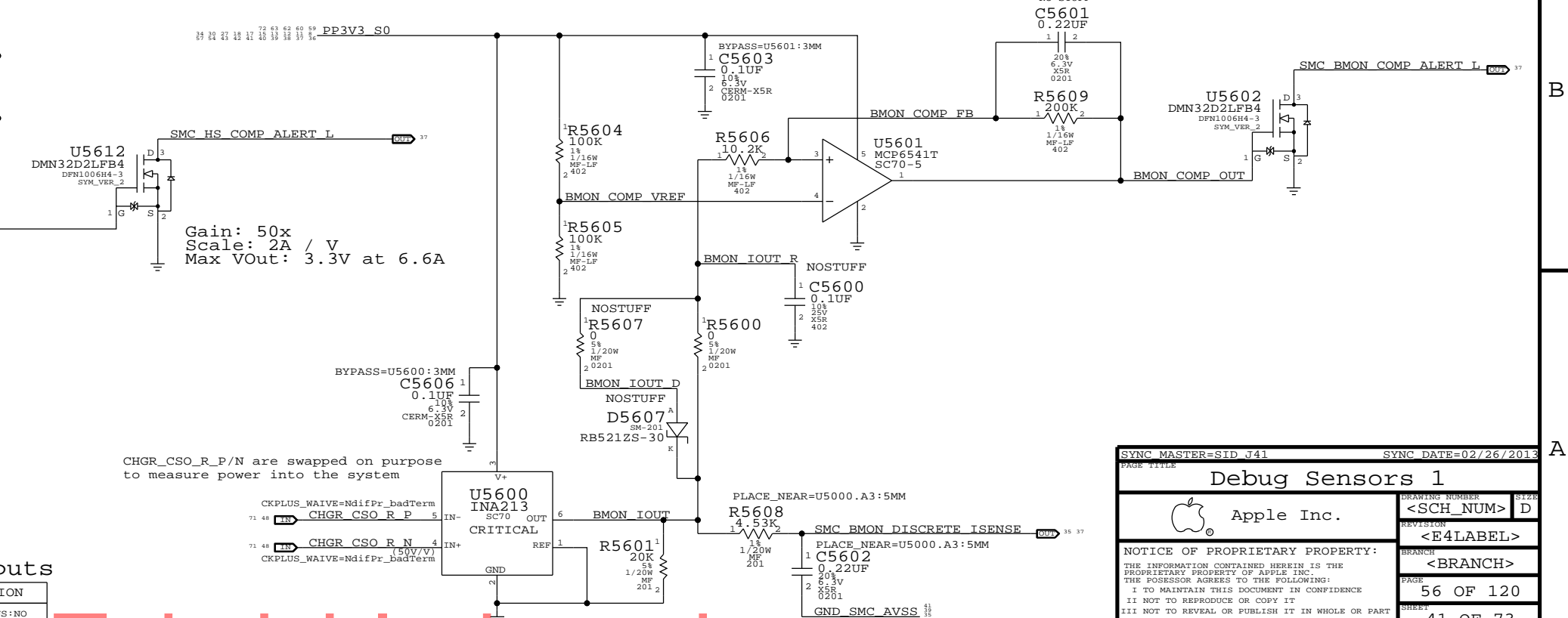
ILDC :LCD Panel Current Sense / Filter



Discrete High side Current threshold



BMON : Discrete BMON Current Sense / Filter



Replacing caps with 100K PD on ISENSE SMC inputs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES,MP,1/20W,100K OHM,5,0201,SMD	C5675		PANEL_ISNS:NO

SYNC MASTER=SID J41

SYNC DATE=02/26/2013

Debug Sensors 1

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DRAWING NUMBER

<SCH_NUM>

REVISION

<E4LABEL>

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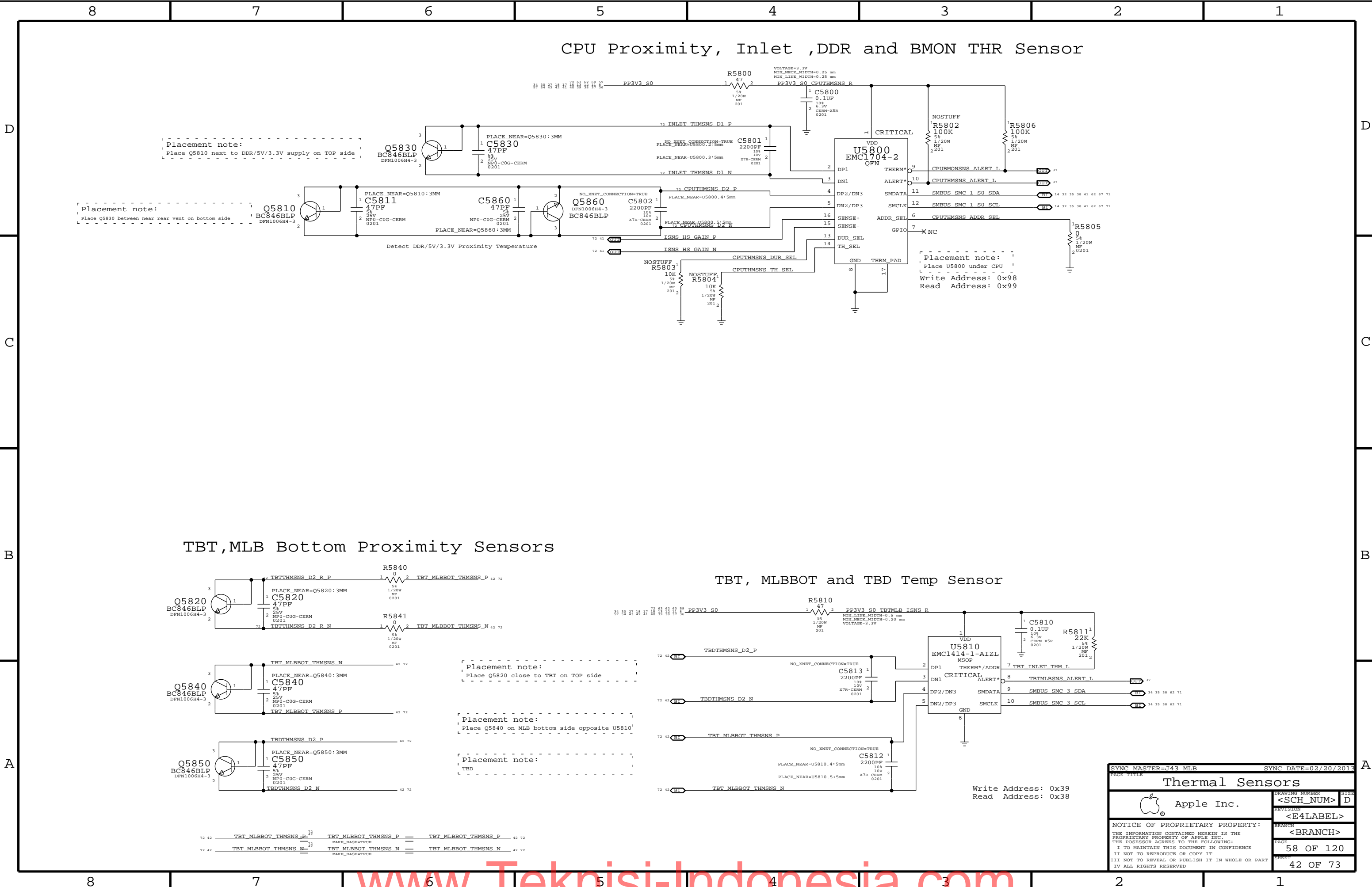
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
SHEET

41 OF 73

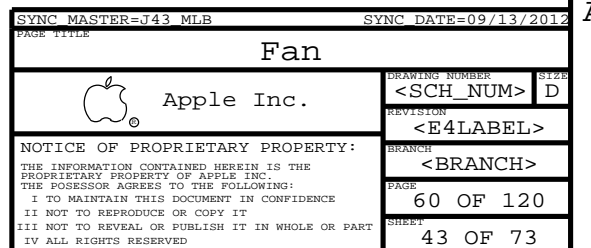


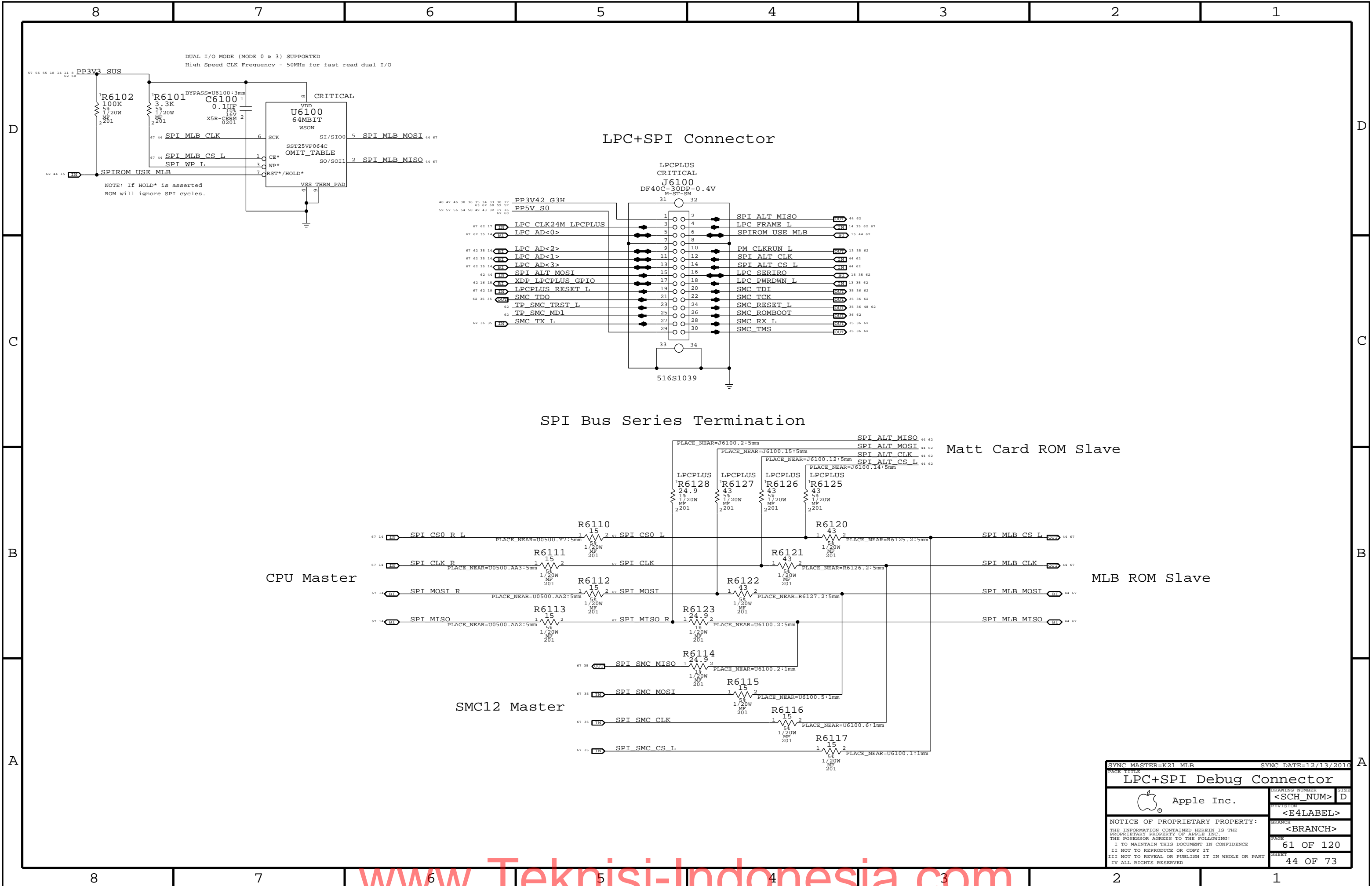
TBT,MLB Bottom Proximity Sensors

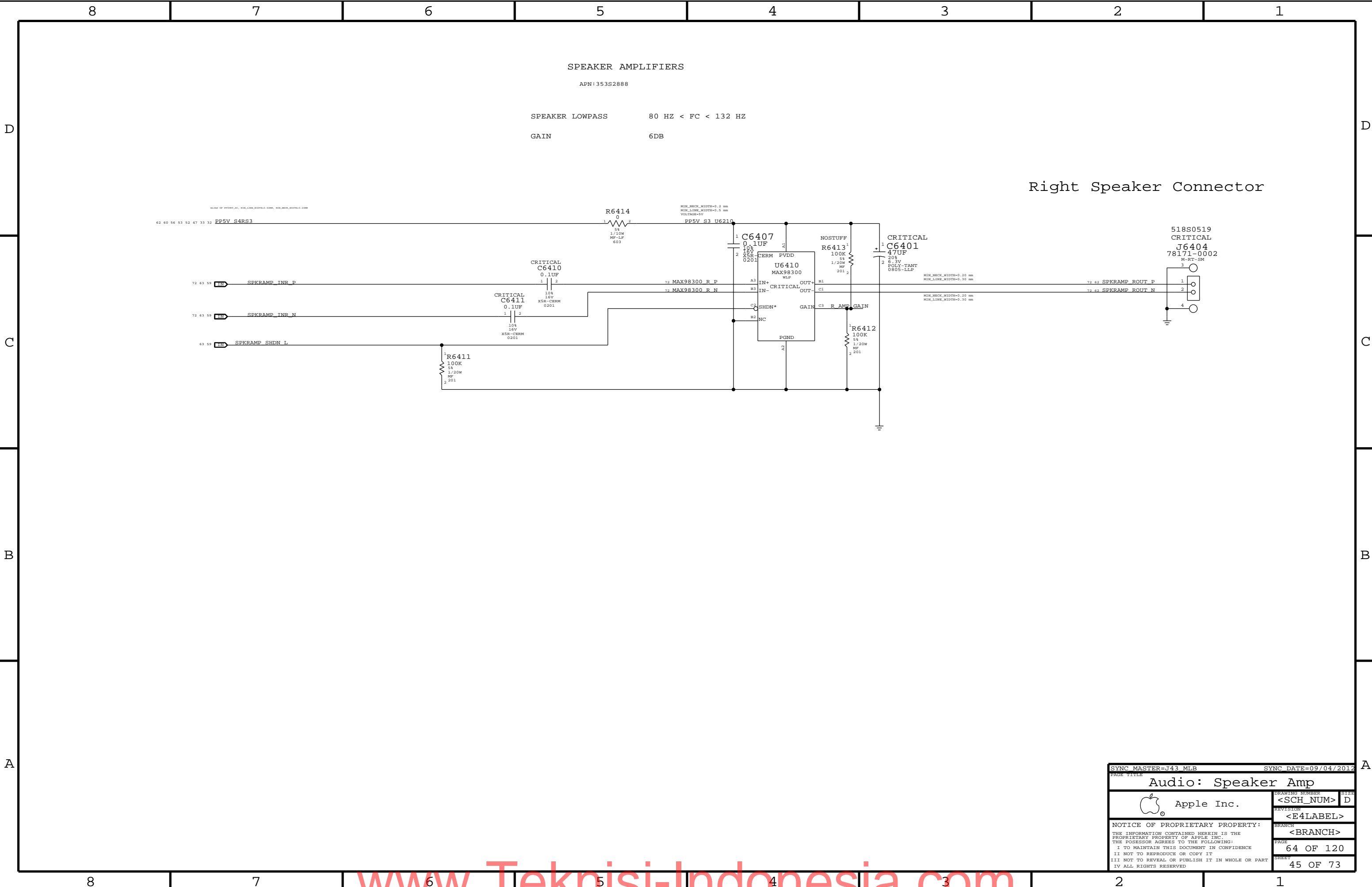
TBT, MLBBOT and TBD Temp Sensor


SYNC MASTER=J43 MLB		SYNC DATE=02/20/2013	
PAGE TITLE			
Thermal Sensors			
 Apple Inc.		DRAWING NUMBER	SIZE
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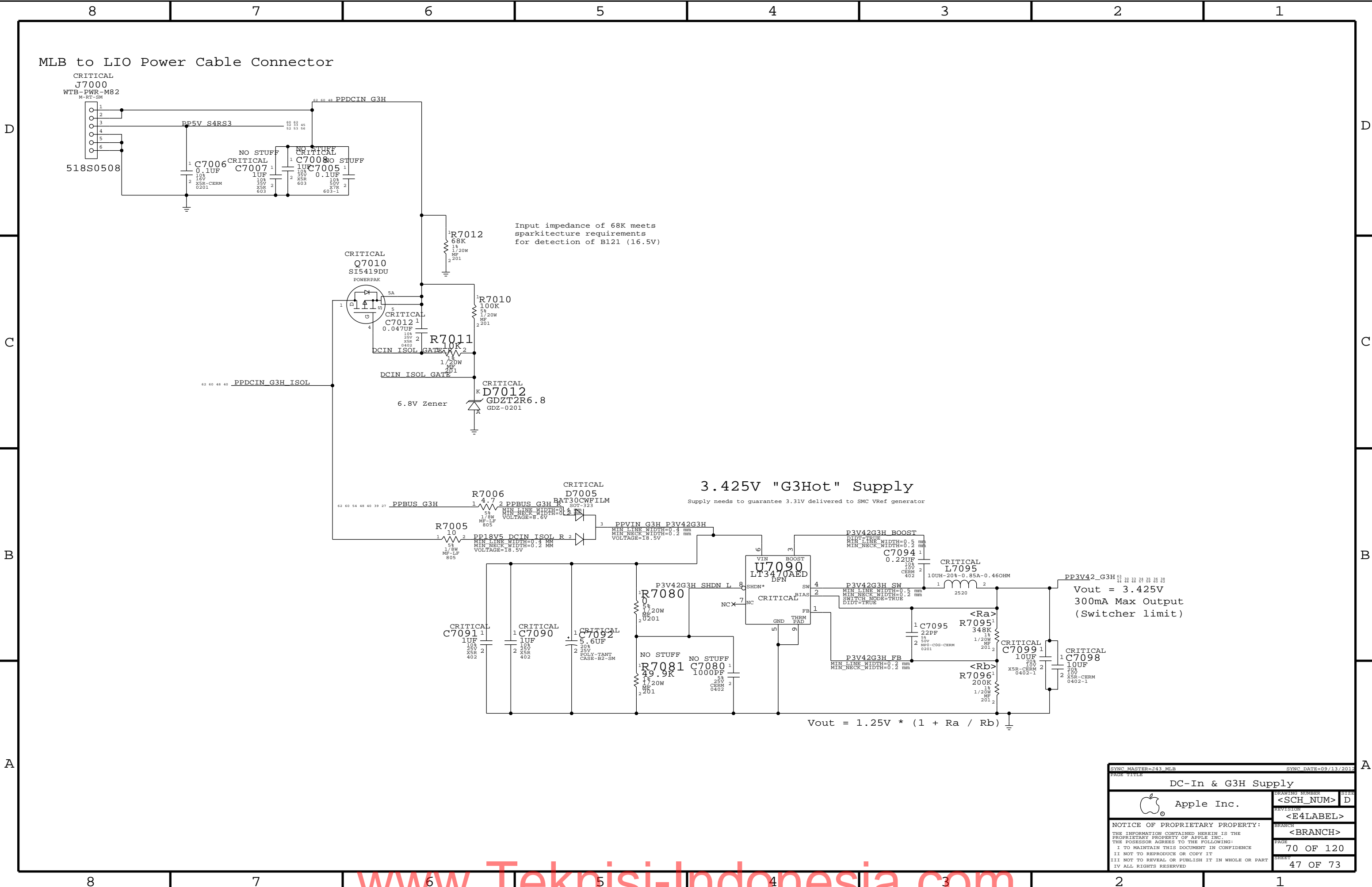
www.Teknisi-Indonesia.com







SYNC MASTER=J43 MLB		SYNC DATE=09/04/2012	
PAGE TITLE			
Audio: Speaker Amp			
 Apple Inc.		DRAWING NUMBER	SIZE
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
Input impedance of 68K meets
sparkiterture requirements
for detection of B121 (16.5V)

3.425V "G3Hot" Supply

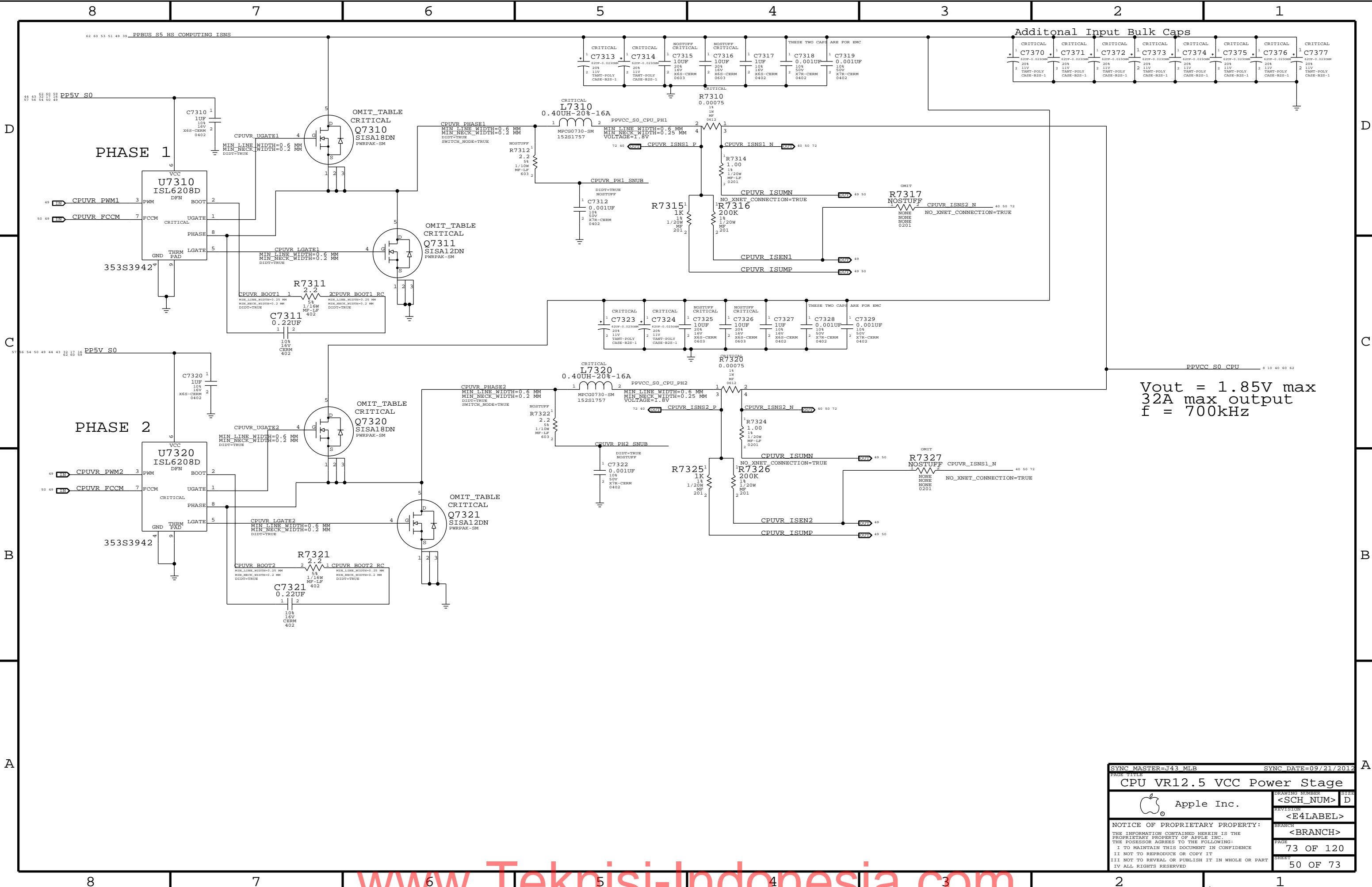
Supply needs to guarantee 3.31V delivered to SMC VRef generator


Vout = 3.425V
300mA Max Output
(Switcher limit)

$$Vout = 1.25V * (1 + Ra / Rb)$$

SYNC MASTER=J43 MLB		SYNC DATE=09/13/2012		
PAGE TITLE				
DC-In & G3H Supply				
	DRAWING NUMBER		SIZE	
	<SCH_NUM>		D	
	REVISION		<E4LABEL>	
	BRANCH		<BRANCH>	
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SYNC MASTER=J43 MLB		SYNC DATE=09/21/2012	
PAGE TITLE			
CPU VR12.5 VCC Power Stage			
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D

C

B

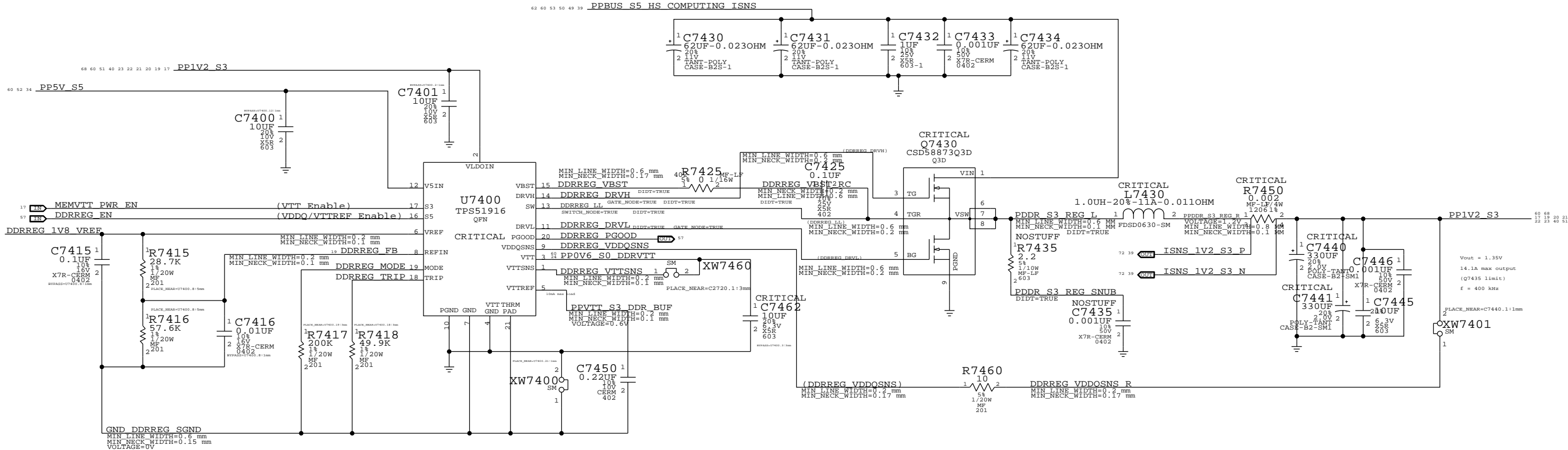
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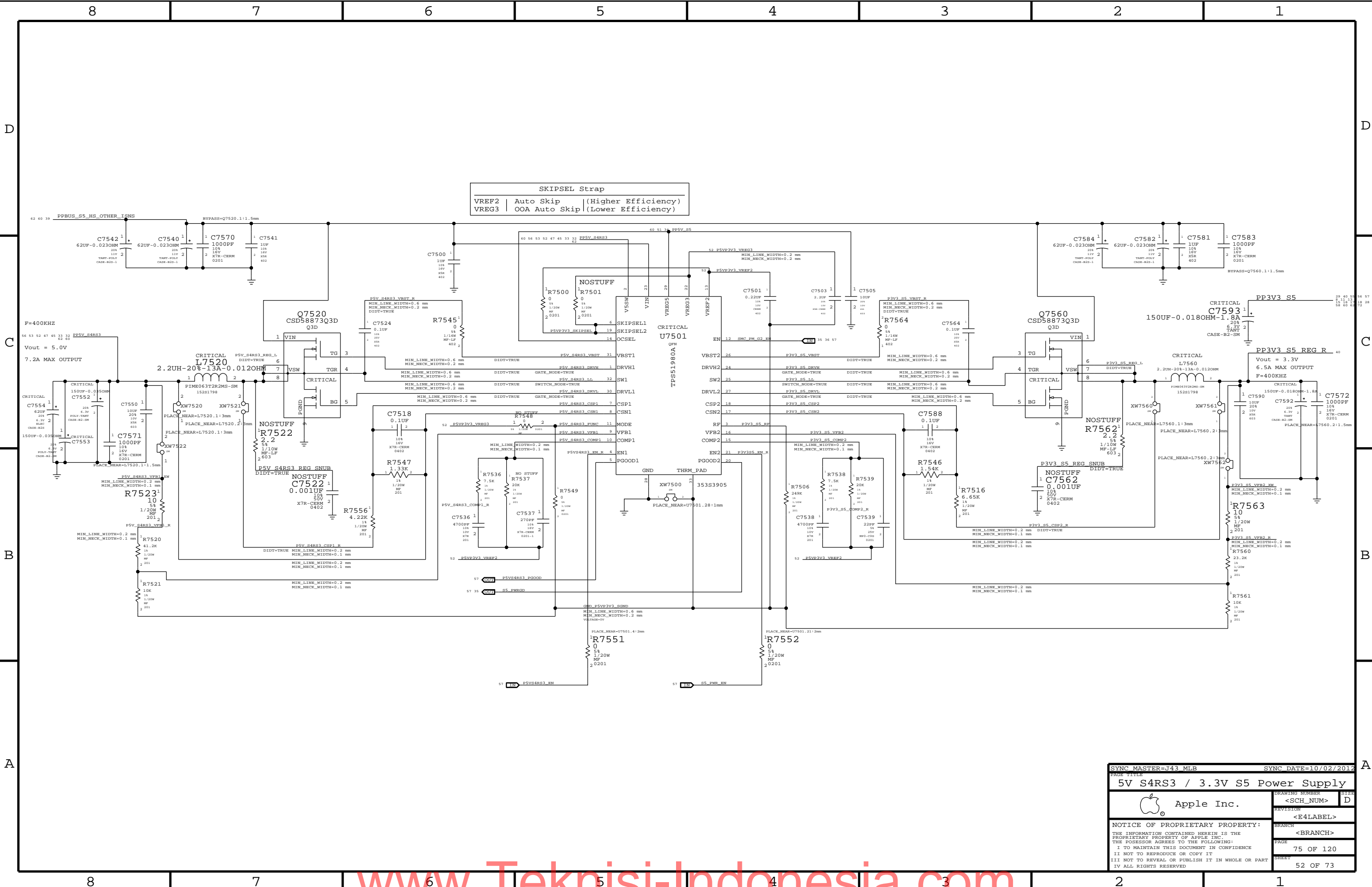
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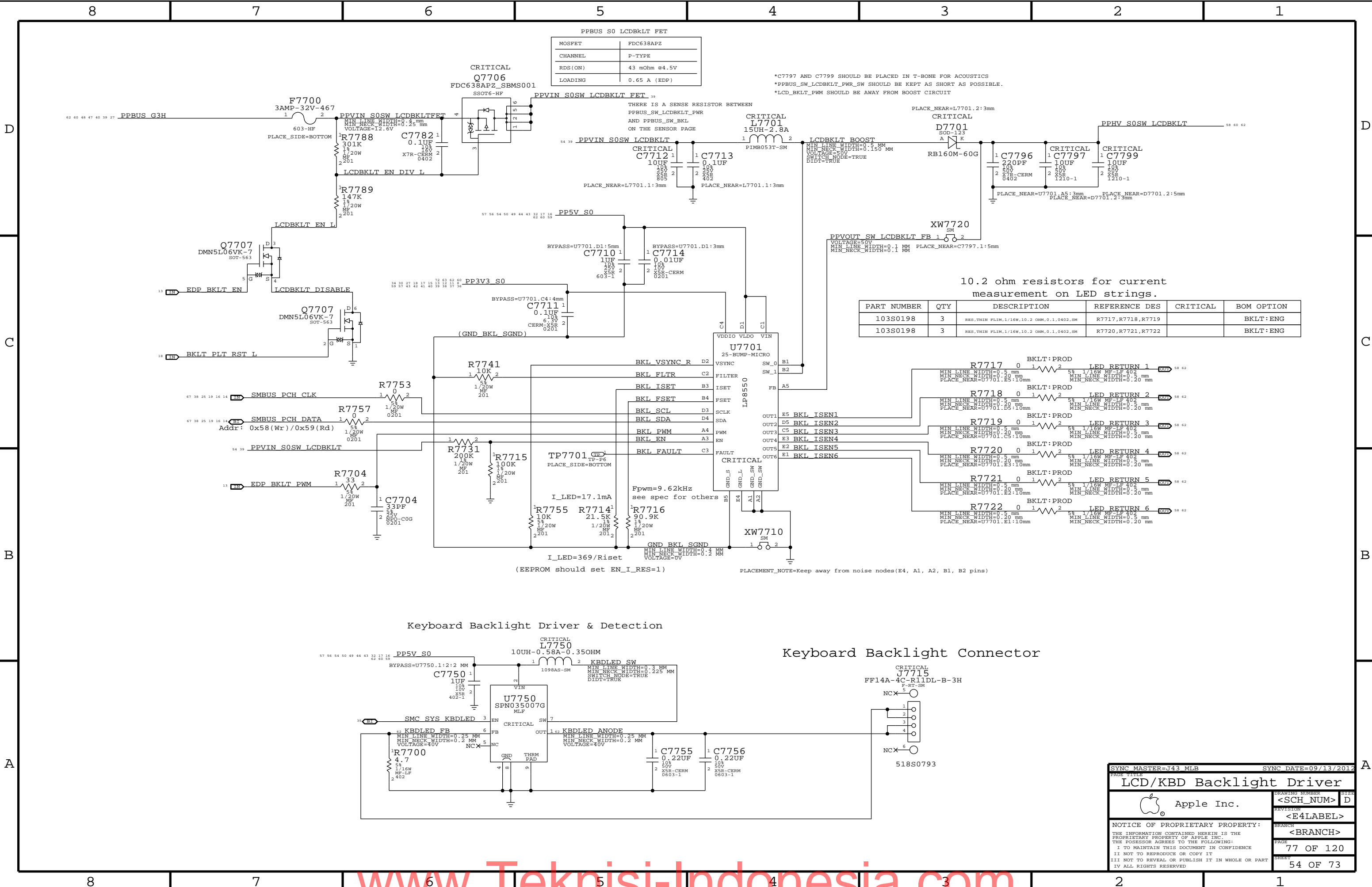
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SYNC MASTER=J43 MLB		SYNC DATE=09/17/2012	
PAGE TITLE			
LPDDR3 Supply			
 Apple Inc.	DRAWING NUMBER	SIZE	
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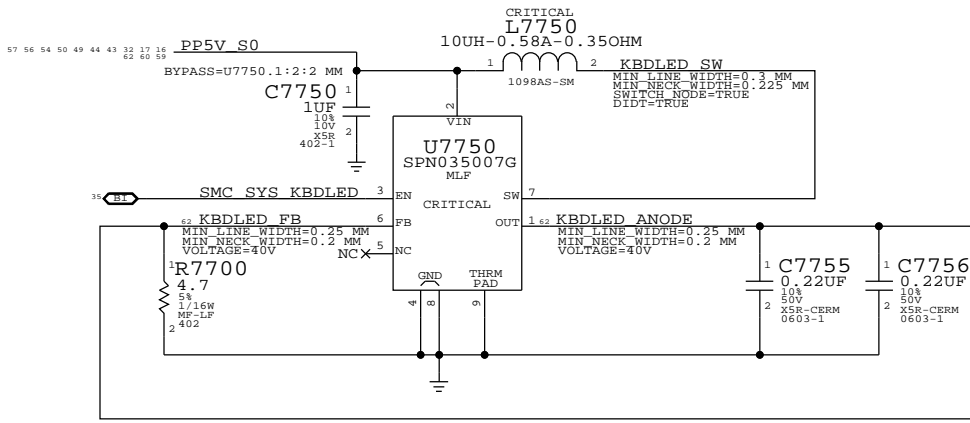
PPBUS S0 LCDBKLT FET	
MOSFET	FDC638APZ
CHANNEL	P-TYPE
RDS(ON)	43 mOhm @4.5V
LOADING	0.65 A (EDP)

*C7797 AND C7799 SHOULD BE PLACED IN T-BONE FOR ACOUSTICS
*PPBUS_SW_LCDBKLT_PWR_SW SHOULD BE KEPT AS SHORT AS POSSIBLE.
*LCD_BKLT_PWM SHOULD BE AWAY FROM BOOST CIRCUIT

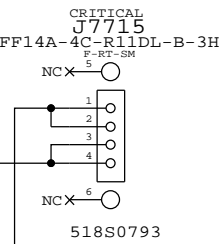
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
103S0198	3	RES,THIN FLIM,1/16W,10.2 OHM,0.1,0402,SM	R7717,R7718,R7719		BKLT:ENG
103S0198	3	RES,THIN FLIM,1/16W,10.2 OHM,0.1,0402,SM	R7720,R7721,R7722		BKLT:ENG

10.2 ohm resistors for current measurement on LED strings.

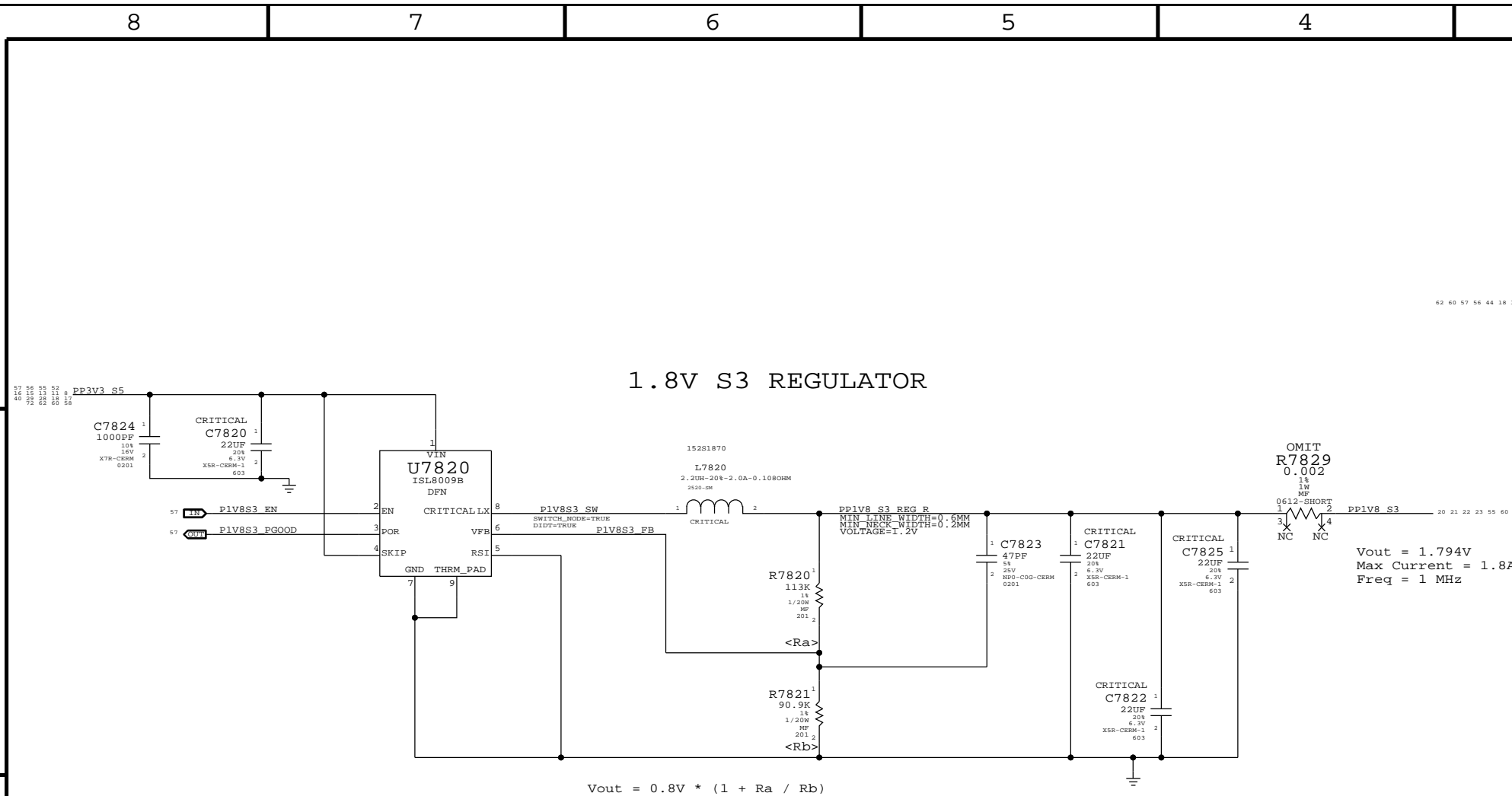
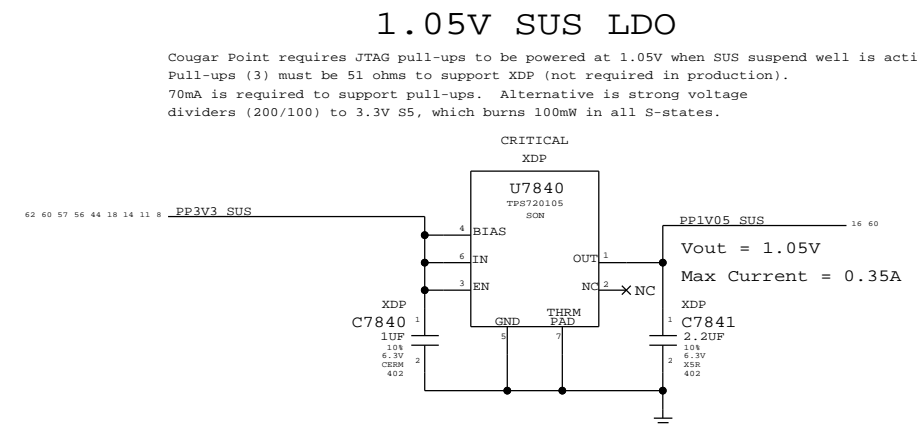
Keyboard Backlight Driver & Detection



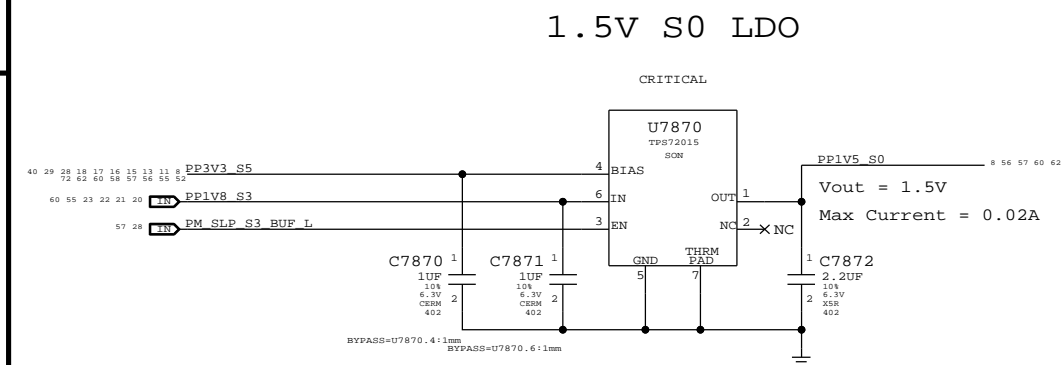
Keyboard Backlight Connector




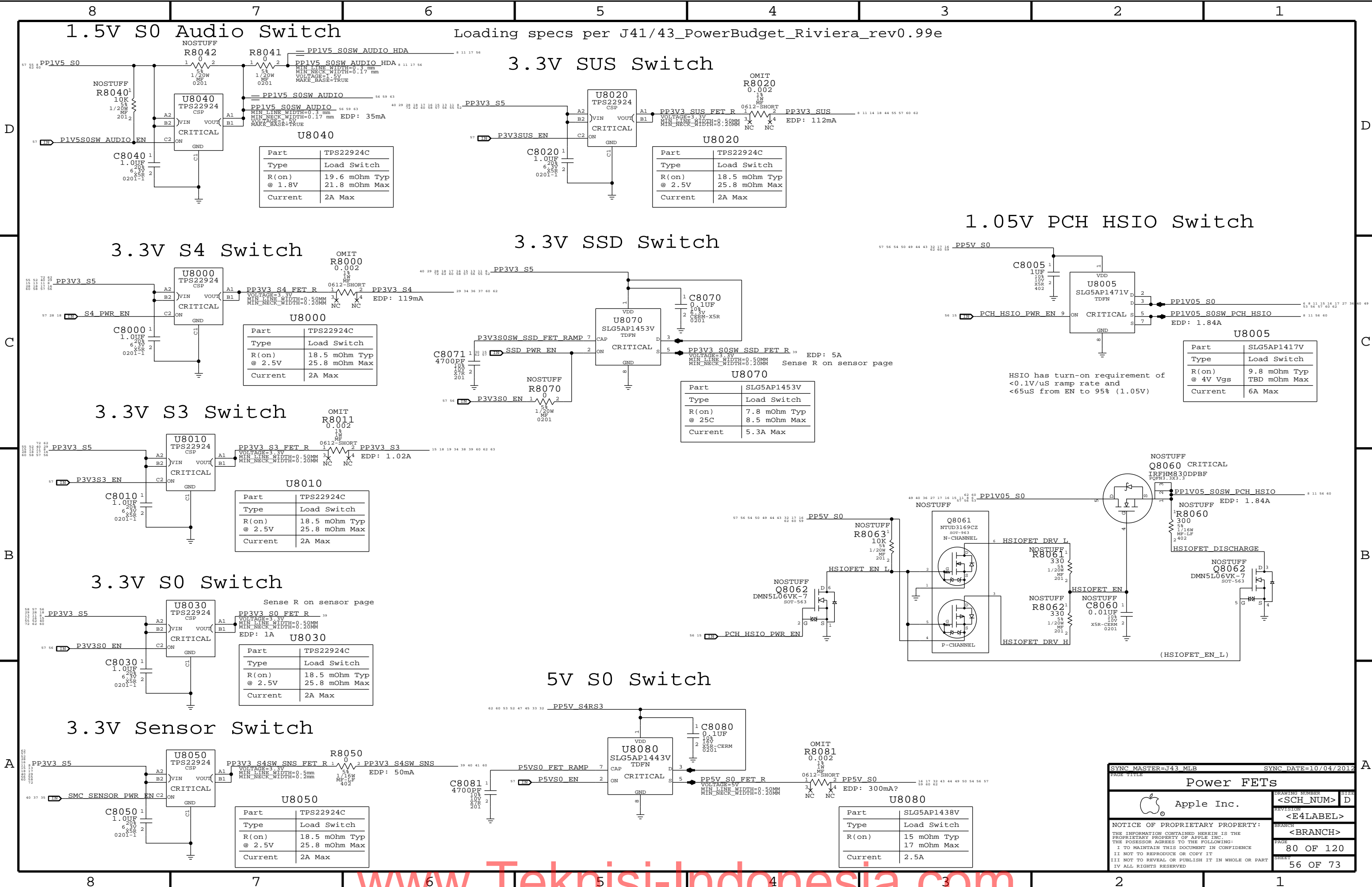
SYNC MASTER=J43 MLB		SYNC DATE=09/13/2012	
PAGE TITLE		LCD/KBD Backlight Driver	
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$$V_{out} = 0.8V * (1 + R_a / R_b)$$


Vout = 1.794V
Max Current = 1.8A
Freq = 1 MHz



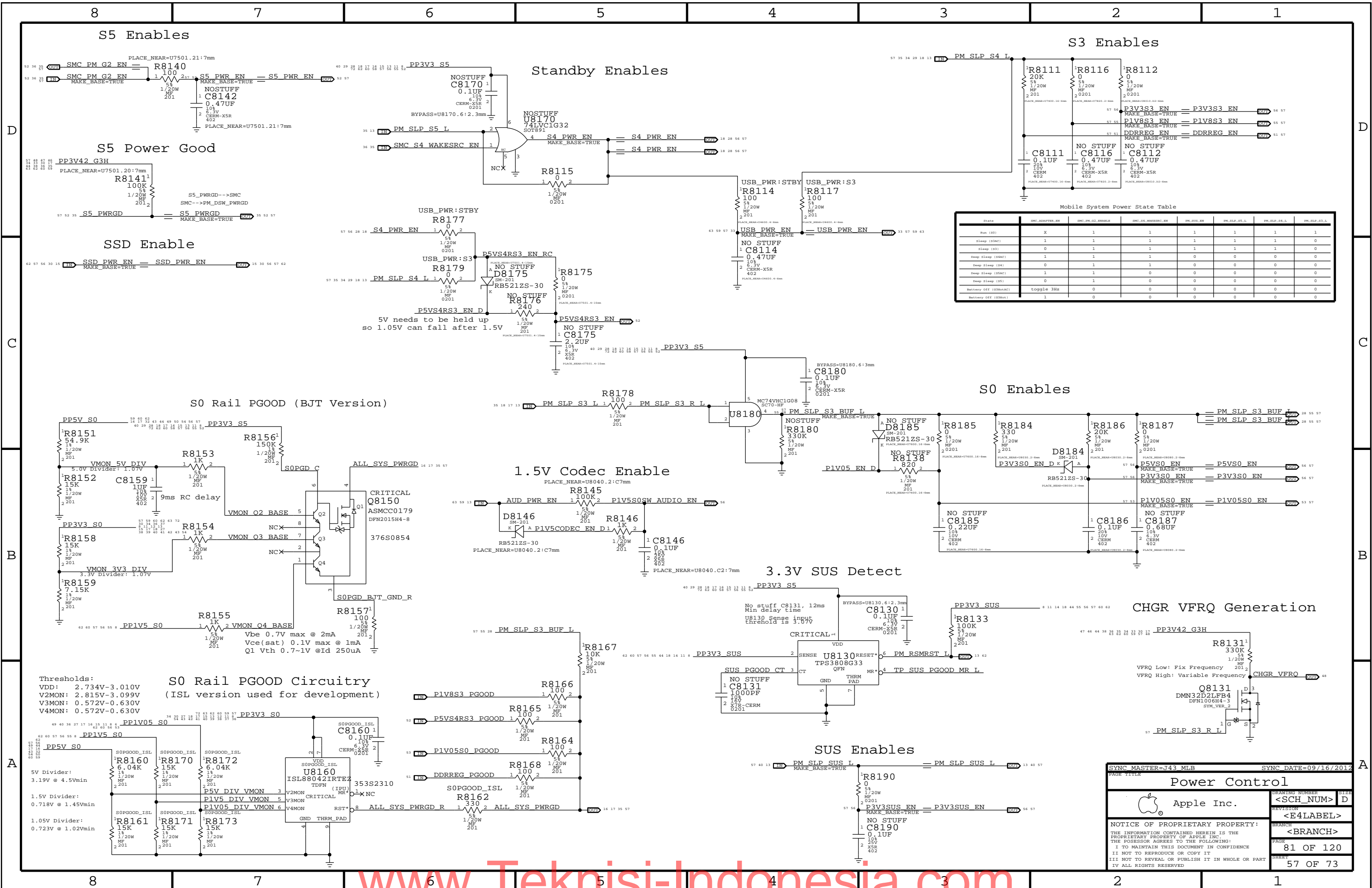
SYNC MASTER=J43 MLB		SYNC DATE=10/04/2012	
PAGE TITLE			
Misc Power Supplies			
	Apple Inc.	DRAWING NUMBER	SIZE
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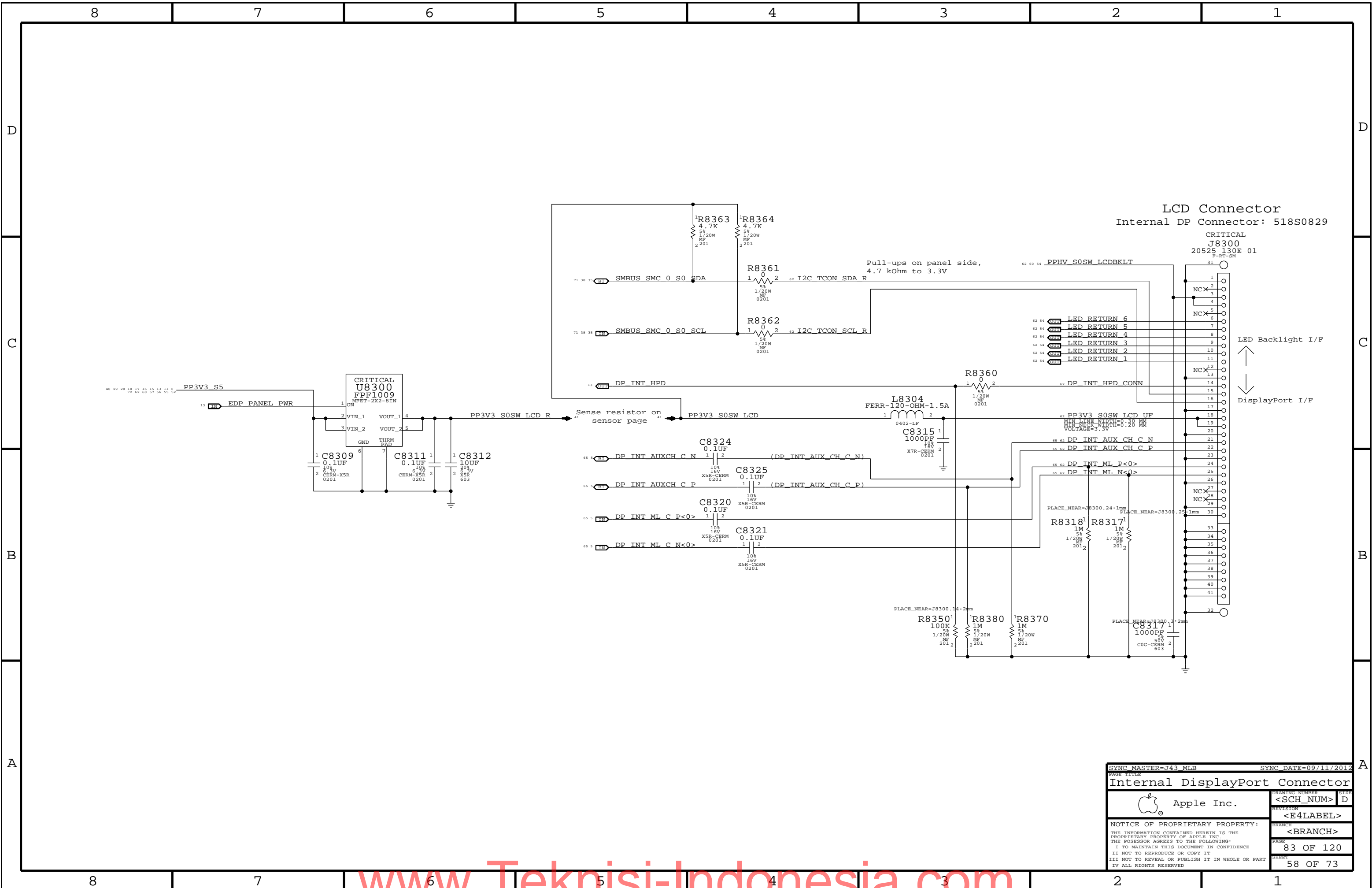



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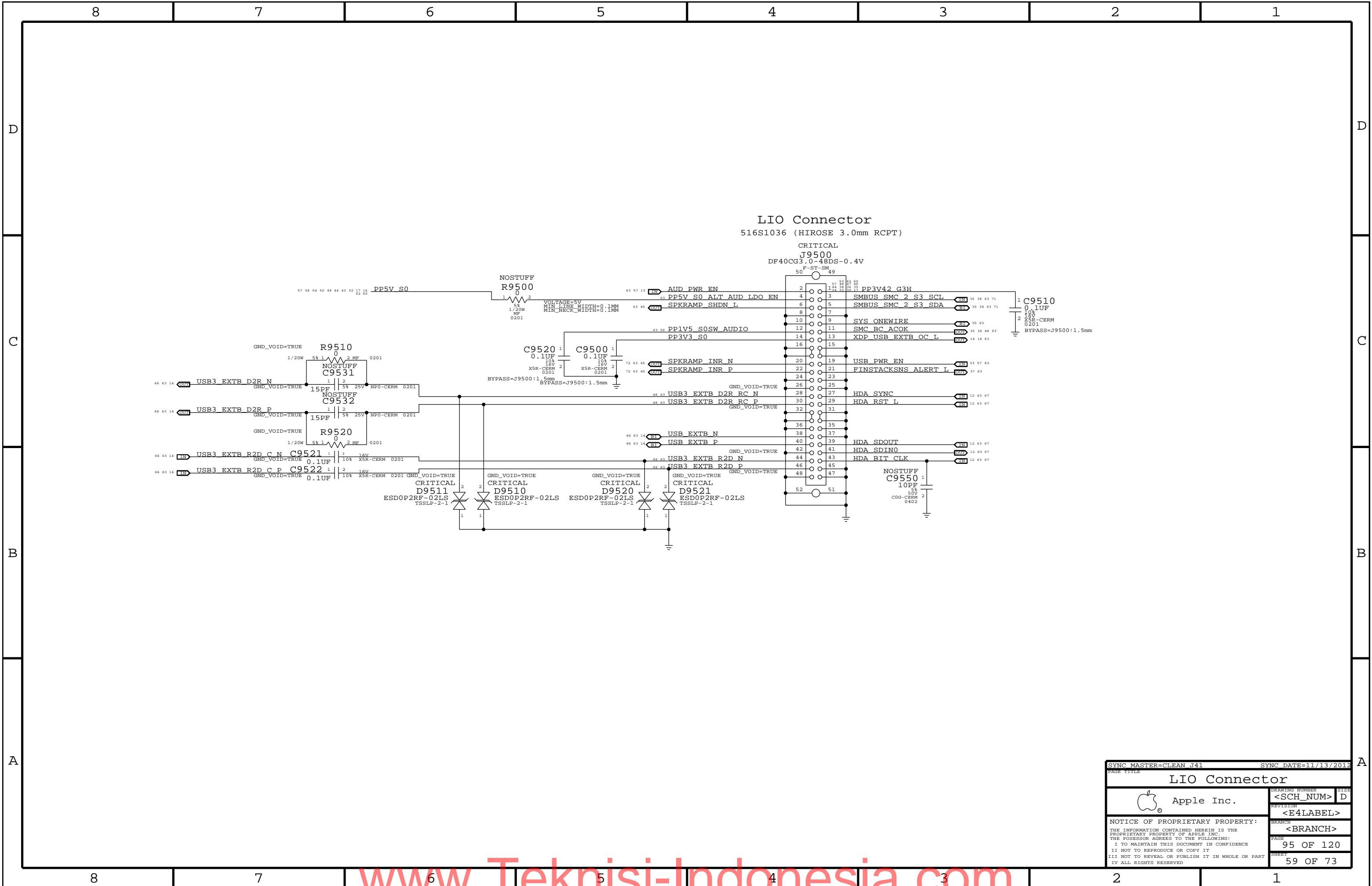
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Power FETs		DRAWING NUMBER	SIZE
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PAGE TITLE			
Internal DisplayPort Connector			
 Apple Inc.		DRAWING NUMBER	
		<SCH_NUM>	
		D	
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SYNC_MASTER=CLEAN J41		SYNC_DATE=11/13/2012	
PAGE TITLE			
LIO Connector			
 Apple Inc.	DRAWING NUMBER		SIZE
	<SCH_NUM>		D
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8	7	6	5	4	3	2	1
LPDDR3 Command/Address							
Memory Bit/Byte Swizzle							
D	MAKE_BASE		MAKE_BASE		MAKE_BASE		
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	=MEM A A<11>		=MEM A DQ<7>		=MEM B DQ<7>		
	=MEM A A<15>		=MEM A DQ<8>		=MEM B DQ<8>		
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TP LPDDR3 RSVD3							
TP LPDDR3 RSVD4							
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=MEM B DOS N<5>							
=MEM B DOS P<6>							
=MEM B DOS N<6>							

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SYNC MASTER=MASTER		SYNC DATE=MASTER	
Signal Aliases			
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8	7	6	5	4	3	2	1
Functional Test Points							
J3501: AirPort / BT Connector							
J6000: Fan Connector							
Misc Voltages & Control Signals							
J4800: IPD Flex Connector							
J7000: DC-In Connector							
J6404: Speaker Connector							
J6950: Battery Connector							
J8300: Internal DP Connector							
J6100: LPC+SPI Connector							
J1800: XDP Connector							
J7715: KB BKLt Connector							
J3700: SSD Connector							
J4002: Camera Connector							
NO_TEST Nets							
Unused nets with offpage							
Func Test / No Test							
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Functional Test Points

Power Aliases

NO_TEST Nets

J9500: LIO Connector

FUNC_TEST

Pin	Signal	Function	Notes
1	TRUE	AUD_PWR_EN	13 57 59
2	TRUE	PP5V_S0_ALT_AUD_LDO_EN	59
3	TRUE	SPKRAMP_SHDN_L	45 59
4	TRUE	PP1V5_S0SW_AUDIO	56 59
5	TRUE	PP3V3_S0	59 62 72
6	TRUE	SPKRAMP_INR_N	45 59 72
7	TRUE	SPKRAMP_INR_P	45 59 72
8	TRUE	USB3_EXTB_D2R_RC_N	59 63 66
9	TRUE	USB3_EXTB_D2R_RC_P	59 63 66
10	TRUE	USB_EXTB_N	14 59 66
11	TRUE	USB_EXTB_P	14 59 66
12	TRUE	USB3_EXTB_R2D_N	59 63 66
13	TRUE	USB3_EXTB_R2D_P	59 63 66
14	TRUE	PP3V42_G3H	17 30 32 34 35 36 38 44 46 47
15	TRUE	SMBUS_SMC_2_S3_SCL	48 57 59 60 62 63
16	TRUE	SMBUS_SMC_2_S3_SDA	35 38 59 71
17	TRUE	SYS_ONEWIRE	35 38 59 71
18	TRUE	SYS_ONEWIRE	35 59
19	TRUE	SMC_BC_ACLK	35 36 48 59
20	TRUE	XDP_USB_EXTB_OC_L	14 16 59
21	TRUE	USB_PWR_EN	33 57 59
22	TRUE	FINSTACKSNS_ALERT_L	37 59
23	TRUE	HDA_SYNC	12 59 67
24	TRUE	HDA_RST_L	12 59 67
25	TRUE	HDA_SDOUT	12 59 67
26	TRUE	HDA_SDIN0	12 59 67
27	TRUE	HDA_BIT_CLK	12 59 67

(Need to add 5 GND TFs)

```
NO_TEST
MAKE_BASE
```

66	63	14	NC USB3RPCIE SD D2RP	==	TRUE	TRUE	NC USB3RPCIE SD D2RP	14	63	86	CPU/PCH
66	63	14	NC USB3RPCIE SD D2RN	==	TRUE	TRUE	NC USB3RPCIE SD D2RN	14	63	86	
66	63	14	NC USB3RPCIE SD R2D CP	==	TRUE	TRUE	NC USB3RPCIE SD R2D CP	14	63	86	
66	63	14	NC USB3RPCIE SD R2D CN	==	TRUE	TRUE	NC USB3RPCIE SD R2D CN	14	63	86	
63	37	35	NC SMC ADC16	==	TRUE	TRUE	NC SMC ADC16	35	37	86	SMC


Bead Probes

06:59:14	USB3_EXTB_D2R_N	TPD	SM	BEAD-PROBE	BPA5111
06:59:14	USB3_EXTB_D2R_P	TPD	SM	BEAD-PROBE	BPA5110
06:59:19	USB3_EXTB_D2R_RC_N	TPD	SM	BEAD-PROBE	BPA5120
06:59:19	USB3_EXTB_D2R_RC_P	TPD	SM	BEAD-PROBE	BPA5201
06:59:14	USB3_EXTB_R2D_C_N	TPD	SM	BEAD-PROBE	BPA5113
06:59:14	USB3_EXTB_R2D_C_P	TPD	SM	BEAD-PROBE	BPA5122
06:59:19	USB3_EXTB_R2D_N	TPD	SM	BEAD-PROBE	BPA5233
06:59:19	USB3_EXTB_R2D_P	TPD	SM	BEAD-PROBE	BPA5232

Unused nets with offpage

(Nets with offpages not used on this project)

SD RESET L	15
XDP SDCONN STATE CHANGE_L	15 16
SD PWR EN	15

SYMC MASTER-MASTER		SYMC DATE-MASTER	
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Project FCT/NC/Aliases			
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CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	0.100 MM	0.100 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?
CPU_AGTL	*	=STANDARD	?

Note: CPU_8MIL and CPU_ITP can be converted back to TABLE_SPACING_RULE once rdar://10308147 is resolved

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_S
CPU_8MIL	*	*	CPU_8MIL_2AN

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_8MIL_2ANY	*	8 MIL	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SELECTOR
CPU_ITP	*	*	CPU_ITP_2ANY

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_ITP_2ANY	*	=4x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SELECTOR
CPU_COMP	CPU_COMP	*	CPU_COMP_2SE
CPU_COMP	*	*	CPU_COMP_2OTH

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_COMP_2SELF	TOP, BOTTOM	=6x_DIELECTRIC	?
CPU_COMP_2OTHER	TOP, BOTTOM	=10x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_COMP_2SELF	*	=4x_DIELECTRIC	?
CPU_COMP_2OTHER	*	=6x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_VCCSENSE	CPU_VCCSENSE	*	CPU_VCCSENSE_2SE
CPU_VCCSENSE	*	*	CPU_VCCSENSE_20TH

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_VCCSENSE_2SELF	TOP, BOTTOM	=6x_DIELECTRIC	?
CPU_VCCSENSE_2OTHER	TOP, BOTTOM	=10x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_VCCSENSE_2SELF	*	=4x_DIELECTRIC	?
CPU_VCCSENSE_2OTHER	*	=6x_DIELECTRIC	?

PCI-Express Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF
CLK_PCIE_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

PCIE Clock Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SEQ
CLK_PCIE	CLK_PCIE	*	CLK_PCIE_2SE
CLK_PCIE	*	*	CLK_PCIE_20TH

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCIE_2SELF	TOP, BOTTOM	=6x_DIELECTRIC	?
CLK_PCIE_2OTHER	TOP, BOTTOM	=10x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCIE_2SELF	*	=4x_DIELECTRIC	?
CLK_PCIE_2OTHER	*	=6x_DIELECTRIC	?

CPU PCIe Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SH
PCIE_CPU_TX	PCIE_CPU_TX	*	PCIE_TX2TX
PCIE_CPU_RX	PCIE_CPU_RX	*	PCIE_RX2RX
PCIE_CPU_TX	*_CPU_TX	*	PCIE_TX2OTHER
PCIE_CPU_RX	*_CPU_RX	*	PCIE_RX2OTHER
PCIE_CPU_TX	*_CPU_RX	*	PCIE_TX2RX
PCIE_CPU_RX	*_CPU_TX	*	PCIE_RX2TX
PCIE_CPU_TX	*_TX	*	PCIE_2OTHERH
PCIE_CPU_RX	*_TX	*	PCIE_2OTHERH
PCIE_CPU_TX	*_RX	*	PCIE_2OTHERH
PCIE_CPU_RX	*_RX	*	PCIE_2OTHERH
PCIE_CPU_TX	*	*	PCIE_2OTHER
PCIE_CPU_RX	*	*	PCIE_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_TX2TX	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_RX2RX	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_TX20THERTX	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_RX20THERRX	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_TX2RX	TOP,BOTTOM	=7x_DIELECTRIC	?
PCIE_RX2TX	TOP,BOTTOM	=7x_DIELECTRIC	?
PCIE_20THERHS	TOP,BOTTOM	=6x_DIELECTRIC	?
PCIE_20THER	TOP,BOTTOM	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_TX2TX	*	=2.5x_DIELECTRIC	?
PCIE_RX2RX	*	=2.5x_DIELECTRIC	?
PCIE_TX2OTHERTX	*	=4x_DIELECTRIC	?
PCIE_RX2OTHERRX	*	=4x_DIELECTRIC	?
PCIE_TX2RX	*	=6x_DIELECTRIC	?
PCIE_RX2TX	*	=6x_DIELECTRIC	?
PCIE_20OTHERHS	*	=4x_DIELECTRIC	?
PCIE_20OTHER	*	=3x_DIELECTRIC	?

PCH PCIE Spacing			
NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_S1
PCIE_PCH_TX	PCIE_PCH_TX	*	PCIE_TX2TX
PCIE_PCH_RX	PCIE_PCH_RX	*	PCIE_RX2RX
PCIE_PCH_TX	*_PCH_TX	*	PCIE_TX2OTHER
PCIE_PCH_RX	*_PCH_RX	*	PCIE_RX2OTHER
PCIE_PCH_TX	*_PCH_RX	*	PCIE_TX2RX
PCIE_PCH_RX	*_PCH_TX	*	PCIE_RX2TX
PCIE_PCH_TX	*_TX	*	PCIE_20THERH
PCIE_PCH_RX	*_TX	*	PCIE_20THERH
PCIE_PCH_TX	*_RX	*	PCIE_20THERH
PCIE_PCH_RX	*_RX	*	PCIE_20THERH
PCIE_PCH_TX	*	*	PCIE_20THER
PCIE_PCH_RX	*	*	PCIE_20THER

Note: DisplayPort tables are on Page 113


SOURCE: 471984_Chief_River_MS_PDG_1.0 and the spacing rule is adjusted per SI team feedback.

CPU Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		PHYSICAL	SPACING	
	CPU_PRCI	CPU_45S	CPU_COMP	CPU_PECI 4 36
	PM_SYNC	CPU_45S	CPU_AGTL	PM_SYNC
	PM_MEM_PWRGD	CPU_45S	CPU_AGTL	PM_MEM_PWRGD
		CPU_45S	CPU_ITP	XDP_DBRESET_L 16 17
		CPU_45S	CPU_ITP	XDP_CPU_PRRY_L 6 16 62
		CPU_45S	CPU_ITP	XDP_CPU_PREQ_L 6 16 62
		CPU_27P4S	CPU_COMP	EDP_COMP
		CPU_27P4S	CPU_COMP	CPU_PEG_COMP
	CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<0> 6
	CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<1> 6
	CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<2> 6
		CPU_45S	CPU_ITP	CPU_CFG<11..0> 6 16 62
	CPU_CATERR_L	CPU_45S	CPU_AGTL	CPU_CATERR_L 6 35
		CPU_45S	CPU_AGTL	CPU_VCCIO_SEL
	CPU_BROCHOT_L	CPU_45S	CPU_AGTL	CPU_PROCHOT_L
	CPU_PWRGD	CPU_45S	CPU_AGTL	CPU_PWRGD 6 35 36 49
	PM_THRMTRIP_T	CPU_45S	CPU_AGTL	PM_THRMTRIP_L 15 36
	DMI_CLK100M	CLK_PCTE_80D	CLK_PCTE	DMI_CLK100M_CPU_P
	DMI_CLK100M	CLK_PCTE_80D	CLK_PCTE	DMI_CLK100M_CPU_N
	DP_L1_REF_CLK120M	CLK_PCTE_80D	CLK_PCTE	DP_L1_REF_CLKP
	DP_L1_REF_CLK120M	CLK_PCTE_80D	CLK_PCTE	DP_L1_REF_CLKN
	ITPCPU_CLK100M	CLK_PCTE_80D	CLK_PCTE	ITPCPU_CLK100M_P
	ITPCPU_CLK100M	CLK_PCTE_80D	CLK_PCTE	ITPCPU_CLK100M_N
	ITPXDPU_CLK100M	CLK_PCTE_80D	CLK_PCTE	ITPXDPU_CLK100M_P
	ITPXDPU_CLK100M	CLK_PCTE_80D	CLK_PCTE	ITPXDPU_CLK100M_N
	ITPXDPU_CLK100M	CLK_PCTE_80D	CLK_PCTE	XDP_CPU_CLK100M_P
	ITPXDPU_CLK100M	CLK_PCTE_80D	CLK_PCTE	XDP_CPU_CLK100M_N
	XDP_TDI	CPU_45S	CPU_ITP	XDP_CPU_TDI 6 16 62
	XDP_TDO	CPU_45S	CPU_ITP	XDP_CPU_TDO 6 16 62
	XDP_TMS	CPU_45S	CPU_ITP	XDP_CPU_TMS 6 16 62
	XDP_TCK	CPU_45S	CPU_ITP	XDP_CPU_TCK 6 16 62
	XDP_TRST_L	CPU_45S	CPU_ITP	XDP_CPUCH_TRST_L 6 12 16 62
	XDP_BPM_L	CPU_45S	CPU_ITP	XDP_BPM_L<1..0> 6 16
		CPU_45S	CPU_ITP	XDP_BPM_L<7..2> 6 16
		CPU_45S	CPU_ITP	XDP_OBSDATA_B<3..0>
		CPU_45S	CPU_ITP	CPU_CFG<15..12> 6 16
	(FSB_CFUURST_L)	CPU_45S	CPU_ITP	XDP_CFUURST_L 16
	CPU_VCCSENSE	SENSE_1T01_P2MM	CPU_VCCSENSE	CPU_VCCSENSE_P 8 49
	CPU_VCCSENSE	SENSE_1T01_P2MM	CPU_VCCSENSE	CPU_VCCSENSE_N 8 49
	CPU_VCCIOSENSE	SENSE_1T01_P2MM	CPU_VCCSENSE	CPU_VCCIOSENSE_P
	CPU_VCCIOSENSE	SENSE_1T01_P2MM	CPU_VCCSENSE	CPU_VCCIOSENSE_N
	CPU_AXG_SENSE	SENSE_1T01_P2MM	CPU_VCCSENSE	CPU_AXG_SENSE_P
	CPU_AXG_SENSE	SENSE_1T01_P2MM	CPU_VCCSENSE	CPU_AXG_SENSE_N
	CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VDDO_SENSE_P
	CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VDDO_SENSE_N
	CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_P
	CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_N
	CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_P
	CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_N
	CPU_VIDALERT_L	CPU_45S	CPU_COMP	CPU_VIDALERT_L 8 49
	CPU_SVIDSCCLK	CPU_45S	CPU_COMP	CPU_VIDSCCLK 8 49
	CPU_SVIDSOUT	CPU_45S	CPU_COMP	CPU_VIDSOUT 8 49
	PCIE_CPU_SSD_R2D	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_C_P<3..0> 12 30
	PCIE_CPU_SSD_R2D	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_C_N<3..0> 12 30
		PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_P<3..0> 30 62
		PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_N<3..0> 30 62
		PCIE_80D	PCIE_CPU_RX	PCIE_SSD_R2R_C_P<3..0> 30 62
		PCIE_80D	PCIE_CPU_RX	PCIE_SSD_R2R_C_N<3..0> 30 62
	PCIE_CPU_SSD_D2R	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_R2R_P<3..0> 12 30 62
	PCIE_CPU_SSD_D2R	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_R2R_N<3..0> 12 30 62
	PCIE_CLK100M_SSD	CLK_PCTE_80D	CLK_PCTE	PCIE_CLK100M_SSD_P 12 30 62
	PCIE_CLK100M_SSD	CLK_PCTE_80D	CLK_PCTE	PCIE_CLK100M_SSD_N 12 30 62
1930	DP_TBT_MI	DP_80D	DP_TX	DP_TBTSNK0_ML_P<3..0> 25
1930	DP_TBT_MI	DP_80D	DP_TX	DP_TBTSNK0_ML_N<3..0> 25
1930		DP_80D	DP_TX	DP_TBTSNK0_ML_C_P<3..0> 5 25
1930		DP_80D	DP_TX	DP_TBTSNK0_ML_C_N<3..0> 5 25
1930	DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBTSNK0_AUXCH_P 25
1930	DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBTSNK0_AUXCH_N 25
1930		DP_80D	DP_AUX	DP_TBTSNK0_AUXCH_C_P 13 25
1930		DP_80D	DP_AUX	DP_TBTSNK0_AUXCH_C_N 13 25
1930	DP_TBT_MI	DP_80D	DP_TX	DP_TBTSNK1_M

PCIe SSD

DP

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CPU Constraints			
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SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_ICOMP	*	=4x_DIELECTRIC	?

SOURCE: 471984_Chief_River_MS_PDG_1.0 and the spacing rule is adjusted per SI team feedback.

UART Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
UART_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
UART	*	=2x_DIELECTRIC	?

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.8

USB 3.0 Interface Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_PCH_TX	USB3_PCH_TX	*	USB3_TX2TX	USB3_TX2TX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_PCH_RX	USB3_PCH_RX	*	USB3_RX2RX	USB3_RX2RX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_PCH_TX	*_PCH_TX	*	USB3_TX2OTHERTX	USB3_TX2OTHERTX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_PCH_RX	*_PCH_RX	*	USB3_RX2OTHERRX	USB3_RX2OTHERRX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_PCH_TX	*_PCH_RX	*	USB3_TX2RX	USB3_TX2RX	TOP,BOTTOM	=7x_DIELECTRIC	?
USB3_PCH_RX	*_PCH_TX	*	USB3_RX2TX	USB3_RX2TX	TOP,BOTTOM	=7x_DIELECTRIC	?
USB3_PCH_TX	*_TX	*	USB3_2OTHERHS	USB3_2OTHERHS	TOP,BOTTOM	=6x_DIELECTRIC	?
USB3_PCH_RX	*_RX	*	USB3_2OTHERHS	USB3_2OTHER	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_PCH_TX	*_RX	*	USB3_2OTHERHS				
USB3_PCH_RX	*_RX	*	USB3_2OTHERHS				
USB3_PCH_TX	*	*	USB3_2OTHER				
USB3_PCH_RX	*	*	USB3_2OTHER				

SOURCE: 471984_Cheif_River_MS_PDG_1.0 and the spacing rule is adjusted per SI team feedback.

PCH Net Properties


ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		PHYSICAL	SPACING	
	PCH_SATA_ICOMP		SATA_ICOMP	PCH_SATAICOMP
	USB_HUB1_UP	USB_80D	USB	USB HUB UP P
	USB_HUB1_UP	USB_80D	USB	USB HUB UP N
	USB_BT	USB_80D	USB	USB BT P
	USB_BT	USB_80D	USB	USB BT N
		USB_80D	USB	USB BT CONN P
		USB_80D	USB	USB BT CONN N
		USB_80D	USB	USB BT WAKE P
		USB_80D	USB	USB BT WAKE N
	USB_TPAD	USB_80D	USB	USB TPAD P
	USB_TPAD	USB_80D	USB	USB TPAD N
		USB_80D	USB	USB TPAD CONN P
		USB_80D	USB	USB TPAD CONN N
		USB_80D	USB	TPAD SPI MOSI USB P
		USB_80D	USB	TPAD SPI MISO USB N
	USB_TPAD_M	USB_80D	USB	USB TPAD M P
	USB_TPAD_M	USB_80D	USB	USB TPAD M N
	USB_SDCARD	USB_80D	USB	USB SDCARD P
	USB_SDCARD	USB_80D	USB	USB SDCARD N
		SPI_45S	SPI	TPAD SPI MOSI
		SPI_45S	SPI	TPAD SPI MISO
		SPI_45S	SPI	TPAD SPI CLK
	USB_EXT_A	USB_80D	USB	USB_EXT_A P
	USB_EXT_A	USB_80D	USB	USB_EXT_A N
		UART_45S	UART	SMC_DEBUGPRT_TX_L
		UART_45S	UART	SMC_DEBUGPRT_RX_L
	USB2_EXT_A	USB_80D	USB	USB2_EXT_A_MUXED_P
	USB2_EXT_A	USB_80D	USB	USB2_EXT_A_MUXED_N
	USB2_EXT_A	USB_80D	USB	USB2_EXT_A_MUXED_F_P
	USB2_EXT_A	USB_80D	USB	USB2_EXT_A_MUXED_F_N
	USB3_EXT_A_RX	USB_80D	USB3_PCH_RX	USB3_EXT_A_D2R_P
	USB3_EXT_A_RX	USB_80D	USB3_PCH_RX	USB3_EXT_A_D2R_N
	USB3_EXT_A_TX	USB_80D	USB3_PCH_TX	USB3_EXT_A_R2D_P
	USB3_EXT_A_TX	USB_80D	USB3_PCH_TX	USB3_EXT_A_R2D_N
		USB_80D	USB3_PCH_RX	USB3_EXT_A_D2R_F_P
		USB_80D	USB3_PCH_RX	USB3_EXT_A_D2R_F_N
		USB_80D	USB3_PCH_TX	USB3_EXT_A_R2D_F_P
		USB_80D	USB3_PCH_TX	USB3_EXT_A_R2D_F_N
		USB_80D	USB3_PCH_TX	USB3_EXT_A_R2D_C_P
		USB_80D	USB3_PCH_TX	USB3_EXT_A_R2D_C_N
	USB_EXT_B	USB_80D	USB	USB_EXT_B P
	USB_EXT_B	USB_80D	USB	USB_EXT_B N
	USB3_EXT_B_RX	USB_80D	USB3_PCH_RX	USB3_EXT_B_D2R_P
	USB3_EXT_B_RX	USB_80D	USB3_PCH_RX	USB3_EXT_B_D2R_N
		USB_80D	USB3_PCH_RX	USB3_EXT_B_D2R_RC_P
		USB_80D	USB3_PCH_RX	USB3_EXT_B_D2R_RC_N
	USB3_EXT_B_TX	USB_80D	USB3_PCH_TX	USB3_EXT_B_R2D_P
	USB3_EXT_B_TX	USB_80D	USB3_PCH_TX	USB3_EXT_B_R2D_N
		USB_80D	USB3_PCH_TX	USB3_EXT_B_R2D_C_P
		USB_80D	USB3_PCH_TX	USB3_EXT_B_R2D_C_N
	USB3_SD_RX	USB_80D	USB3_PCH_RX	NC_USB3RPCIE_SD_D2RP
	USB3_SD_RX	USB_80D	USB3_PCH_RX	NC_USB3RPCIE_SD_D2RN
	USB3_SD_TX	USB_80D	USB3_PCH_TX	NC_USB3RPCIE_SD_R2D_CP
	USB3_SD_TX	USB_80D	USB3_PCH_TX	NC_USB3RPCIE_SD_R2D_CN
		USB_80D	USB3_PCH_RX	USB3_SD_D2R_C_P
		USB_80D	USB3_PCH_RX	USB3_SD_D2R_C_N
		USB_80D	USB3_PCH_TX	USB3_SD_R2D_P
		USB_80D	USB3_PCH_TX	USB3_SD_R2D_N
	PCH_USB_RBIAS	PCH_USB_RBIAS		PCH_USB_RBIAS
	PCH_DIFCLK_UNUSED	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_PCH_P
	PCH_DIFCLK_UNUSED	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_PCH_N
	PCH_DIFCLK_UNUSED	CLK_PCIE_80D	CLK_PCIE	PCH_CLK96M_DOT_P
	PCH_DIFCLK_UNUSED	CLK_PCIE_80D	CLK_PCIE	PCH_CLK96M_DOT_N
	PCH_DIFCLK_UNUSED	CLK_PCIE_80D	CLK_PCIE	PCH_CLK100M_SATA_P
	PCH_DIFCLK_UNUSED	CLK_PCIE_80D	CLK_PCIE	PCH_CLK100M_SATA_N
	PCH_DIFCLK_UNUSED	CPU_45S	CLK_PCIE	PCH_CLK14P3M_REFCLK

USB Hucopyb nets

TP SPI nets

USB EXTA nets (Right USB port)

USB EXTB nets (Left USB port)

SYNC MASTER=CLEAN J41		SYNC DATE=11/13/2012	
PAGE TITLE			
PCH Constraints 1			
	Apple Inc.	DRAWING NUMBER	SIZE
		<SCH_NUM>	
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		PAGE	112 OF 120
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LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	=3x_DIELECTRIC	?
CLK_LPC	*	=4x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ixex Peak M (DG-398905-398905_v1.5), Section 3.15

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_45S_R_50S	TOP, BOTTOM	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE		
SMB_45S_R_50S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for IbeX Peak M (DG-398905-398905_v1.5), Section 3.15

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=4x_DIELECTRIC	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	=4x _{DIELECTRIC}	?

XDP Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCH_ITP	*	=2:1_SPACING	?

DisplayPort

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_2DP	*	=3x_DIELECTRIC	?
DP_2OTHERHS	*	=4x_DIELECTRIC	?
DP_2OTHER	*	=3x_DIELECTRIC	?
DP_AUX	*	=3x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DP_TX	DP_TX	*	DP_2DP
DP_TX	*_TX	*	DP_20THERHS
DP_TX	*_RX	*	DP_20THERHS
DP_TX	*	*	DP_20THER

System Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_25M_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
















SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=2x_DIELECTRIC	?
CLK_25M	*	=5x_DIELECTRIC	?


NOTE: 25MHz system clocks very sensitive to noise.

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		PHYSICAL	SPACING	
<div></div>	LPC_AD	LPC_45S	LPC	LPC AD<3..0>14354462
<div></div>	LPC_FRAME_L	LPC_45S	LPC	LPC FRAME_L14354462
<div></div>		LPC_45S	LPC	LPCPLUS RESET_L144462
<div></div>	LPC_CLK33M	CLK LPC_45S	CLK LPC	LPC CLK24M SMC1735
<div></div>		CLK LPC_45S	CLK LPC	LPC CLK24M SMC_R1217
<div></div>	LPC_CLK33M	CLK LPC_45S	CLK LPC	LPC CLK24M LPCPLUS174462
<div></div>		CLK LPC_45S	CLK LPC	LPC CLK24M LPCPLUS_R1217
<div></div>				
<div></div>	SMBUS_PCH_CLK	SMB_45S_R_50S	SMB	SMBUS PCH_CLK141619253854
<div></div>	SMBUS_PCH_DATA	SMB_45S_R_50S	SMB	SMBUS PCH_DATA141619253854
<div></div>	SMBUS_PCH_0_CLK	SMB_45S_R_50S	SMB	SML_PCH_0_CLK1438
<div></div>	SMBUS_PCH_0_DATA	SMB_45S_R_50S	SMB	SML_PCH_0_DATA1438
<div></div>	SMBUS_SMC_1_S0_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_1_S0_SCL14323538414262
<div></div>	SMBUS_SMC_1_S0_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_1_S0_SDA14323538414262
<div></div>				
<div></div>	HDA_BIT_CLK	HDA_45S	HDA	HDA_BIT_CLK125963
<div></div>		HDA_45S	HDA	HDA_BIT_CLK_R12
<div></div>	HDA_SYNC	HDA_45S	HDA	HDA_SYNC125963
<div></div>		HDA_45S	HDA	HDA_SYNC_R12
<div></div>	HDA_RST_L	HDA_45S	HDA	HDA_RST_R_L12
<div></div>		HDA_45S	HDA	HDA_RST_L125963
<div></div>	HDA_SDIN0	HDA_45S	HDA	HDA_SDIN0125963
<div></div>	HDA_SDOOUT	HDA_45S	HDA	HDA_SDOOUT125963
<div></div>		HDA_45S	HDA	HDA_SDOOUT_R1217
<div></div>				
<div></div>	PM_SUS_CLK	CLK_SLOW_45S	CLK_SLOW	PM_CLK32K_SUSCLK_R1336
<div></div>		CLK_SLOW_45S	CLK_SLOW	SMC_CLK32K3536
<div></div>	SPI_CLK	SPT_45S	SPT	SPI_CLK_R1444
<div></div>		SPT_45S	SPT	SPI_CLK44
<div></div>	SPI_MOSI	SPT_45S	SPT	SPI_MOSI_R1444
<div></div>		SPT_45S	SPT	SPI_MOSI44
<div></div>	SPI_MISO	SPT_45S	SPT	SPI_MISO1444
<div></div>		SPT_45S	SPT	SPI_MISO_R44
<div></div>	SPI_CS0	SPT_45S	SPT	SPI_CS0_R_L1444
<div></div>		SPT_45S	SPT	SPI_CS0_L44
<div></div>		SPT_45S	SPT	SPI_SMC_CLK3544
<div></div>		SPT_45S	SPT	SPI_SMC_MOSI3544
<div></div>		SPT_45S	SPT	SPI_SMC_MISO3544
<div></div>		SPT_45S	SPT	SPI_SMC_CS_L3544
<div></div>		SPT_45S	SPT	SPI_MLB_CLK44
<div></div>		SPT_45S	SPT	SPI_MLB_MOSI44
<div></div>		SPT_45S	SPT	SPI_MLB_MISO44
<div></div>		SPT_45S	SPT	SPI_MLB_CS_L44
<div></div>				
<div></div>	PCIE_AP_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_AP_R2D_P2962
<div></div>	PCIE_AP_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_AP_R2D_N2962
<div></div>		PCIE_80D	PCIE_PCH_TX	PCIE_AP_R2D_C_P1429
<div></div>		PCIE_80D	PCIE_PCH_TX	PCIE_AP_R2D_C_N1429
<div></div>	PCIE_AP_D2R	PCIE_80D	PCIE_PCH_RX	PCIE_AP_D2R_P142962
<div></div>	PCIE_AP_D2R	PCIE_80D	PCIE_PCH_RX	PCIE_AP_D2R_N142962
<div></div>	PCIE_CLK100M_AP	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_AP_P122962
<div></div>	PCIE_CLK100M_AP	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_AP_N122962
<div></div>				
<div></div>	PCIE_TBT_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_TBT_R2D_P<3..0>25
<div></div>	PCIE_TBT_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_TBT_R2D_N<3..0>25
<div></div>		PCIE_80D	PCIE_PCH_TX	PCIE_TBT_R2D_C_P<3..0>1425
<div></div>		PCIE_80D	PCIE_PCH_TX	PCIE_TBT_R2D_C_N<3..0>1425
<div></div>	PCIE_TBT_D2R	PCIE_80D	PCIE_PCH_RX	PCIE_TBT_D2R_P<3..0>1425
<div></div>	PCIE_TBT_D2R	PCIE_80D	PCIE_PCH_RX	PCIE_TBT_D2R_N<3..0>1425
<div></div>		PCIE_80D	PCIE_PCH_RX	PCIE_TBT_D2R_C_P<3..0>25
<div></div>		PCIE_80D	PCIE_PCH_RX	PCIE_TBT_D2R_C_N<3..0>25
<div></div>	PCIE_CLK100M_TBT	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_TBT_P1225
<div></div>	PCIE_CLK100M_TBT	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_TBT_N1225
<div></div>				
<div></div>		CLK_PCIE_80D	CLK_PCIE	PEG_CLK100M_P
<div></div>		CLK_PCIE_80D	CLK_PCIE	PEG_CLK100M_N
<div></div>				
<div></div>	XDP_TDI	PCH_45S	PCH_ITP	XDP_PCH_TDI121662
<div></div>	XDP_TDO	PCH_45S	PCH_ITP	XDP_PCH_TDO121662
<div></div>	XDP_TMS	PCH_45S	PCH_ITP	XDP_PCH_TMS121662
<div></div>	XDP_TCK	PCH_45S	PCH_ITP	XDP_PCH_TCK121662
<div></div>				
<div></div>	PCIE_CAM	PCIE_80D	PCIE_PCH_TX	PCIE_CAMERA_R2D_P3132
<div></div>	PCIE_CAM	PCIE_80D	PCIE_PCH_TX	PCIE_CAMERA_R2D_N3132
<div></div>		PCIE_80D	PCIE_PCH_TX	PCIE_CAMERA_R2D_C_P1432
<div></div>		PCIE_80D	PCIE_PCH_TX	PCIE_CAMERA_R2D_C_N1432
<div></div>	PCIE_CAM	PCIE_80D	PCIE_PCH_RX	PCIE_CAMERA_D2R_P1432
<div></div>	PCIE_CAM	PCIE_80D	PCIE_PCH_RX	PCIE_CAMERA_D2R_N1432
<div></div>		PCIE_80D	PCIE_PCH_RX	PCIE_CAMERA_D2R_C_P3132
<div></div>		PCIE_80D	PCIE_PCH_RX	PCIE_CAMERA_D2R_C_N3132
<div></div>	PCIE_CLK100M_CAM	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_CAMERA_P1232
<div></div>	PCIE_CLK100M_CAM	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_CAMERA_N1232
<div></div>		CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_CAMERA_C_P3132
<div></div>		CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_CAMERA_C_N3132

Clock Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		PHYSICAL	SPACING	
	SYSCLK_CLK32K_RTC	CLK_SLOW_45S	CLK_SLOW	SYSCLK_CLK32K_RTCX1
	SYSCLK_CLK25M_SB	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_CAMERA
		CLK_25M_45S	CLK_25M	CLK25M_CAM_CLKP
		CLK_25M_45S	CLK_25M	CLK25M_CAM_XTALP_R
		CLK_25M_45S	CLK_25M	CLK25M_CAM_XTALP
		CLK_25M_45S	CLK_25M	CLK25M_CAM_XTALN
		CLK_25M_45S	CLK_25M	CLK25M_CAM_CLKN
	SYSCLK_CLK25M_TBT	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT
		CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT_R
	SYSCLK_CLK25M_XTAL	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X1
		CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X2
		CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X2_R
		CLK_25M_45S	CLK_25M	SDCLK_CLK25M_X2
		CLK_25M_45S	CLK_25M	SDCLK_CLK25M_X2_R
		CLK_25M_45S	CLK_25M	SDSCLK_CLK25M_X1

SYNC MASTER=J43 MLB		SYNC DATE=09/14/2012	
PAGE TITLE			
PCH Constraints 2			
	Apple Inc.	DRAWING NUMBER	SIZE
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		PAGE	113 OF 120
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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE
MEM_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_73D	*	=73_OHM_DIFF	=73_OHM_DIFF	=73_OHM_DIFF	=73_OHM_DIFF	=73_OHM_DIFF	=73_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_DATA2SELF	*	=2x_DIELECTRIC	?
MEM_DATA2OTHERMEM	*	=8x_DIELECTRIC	?
MEM_QS2OWNDATA	*	=3x_DIELECTRIC	?
MEM_CMD2CMD	*	=3x_DIELECTRIC	?
MEM_CMD2CTRL	*	=3x_DIELECTRIC	?
MEM_CTRL2CTRL	*	=3x_DIELECTRIC	?
MEM_CLK2CLK	*	=6x_DIELECTRIC	?
MEM_2OTHERMEM	*	=4x_DIELECTRIC	?
MEM_2PWR	*	=2x_DIELECTRIC	10000
MEM_2GND	*	=2x_DIELECTRIC	10000
MEM_2OTHER	*	=6x_DIELECTRIC	?

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_PWR	MEM_*	*	MEM_2PWR
MEM_PWR	*	*	DEFAULT

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MEM_70D	MEM_TERM	MEM_73D
MEM_40S	MEM_TERM	MEM_50S

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	MEM_*	*	MEM_2GND

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DQS_0	MEM_A_DATA_0	*	MEM_QS2OWNDATA
MEM_A_DQS_1	MEM_A_DATA_1	*	MEM_QS2OWNDATA
MEM_A_DQS_2	MEM_A_DATA_2	*	MEM_QS2OWNDATA
MEM_A_DQS_3	MEM_A_DATA_3	*	MEM_QS2OWNDATA
MEM_A_DQS_4	MEM_A_DATA_4	*	MEM_QS2OWNDATA
MEM_A_DQS_5	MEM_A_DATA_5	*	MEM_QS2OWNDATA
MEM_A_DQS_6	MEM_A_DATA_6	*	MEM_QS2OWNDATA
MEM_A_DQS_7	MEM_A_DATA_7	*	MEM_QS2OWNDATA
MEM_B_DQS_0	MEM_B_DATA_0	*	MEM_QS2OWNDATA
MEM_B_DQS_1	MEM_B_DATA_1	*	MEM_QS2OWNDATA
MEM_B_DQS_2	MEM_B_DATA_2	*	MEM_QS2OWNDATA
MEM_B_DQS_3	MEM_B_DATA_3	*	MEM_QS2OWNDATA
MEM_B_DQS_4	MEM_B_DATA_4	*	MEM_QS2OWNDATA
MEM_B_DQS_5	MEM_B_DATA_5	*	MEM_QS2OWNDATA
MEM_B_DQS_6	MEM_B_DATA_6	*	MEM_QS2OWNDATA
MEM_B_DQS_7	MEM_B_DATA_7	*	MEM_QS2OWNDATA

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DATA_*	=SAME	*	MEM_DATA2SELF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DATA_*	MEM_*	*	MEM_DATA2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_CTRL	*	MEM_CMD2CTRL
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2CLK

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*	MEM_*	*	MEM_2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DQS_0	*	*	MEM_2OTHER
MEM_A_DQS_1	*	*	MEM_2OTHER
MEM_A_DQS_2	*	*	MEM_2OTHER
MEM_A_DQS_3	*	*	MEM_2OTHER
MEM_A_DQS_4	*	*	MEM_2OTHER
MEM_A_DQS_5	*	*	MEM_2OTHER
MEM_A_DQS_6	*	*	MEM_2OTHER
MEM_A_DQS_7	*	*	MEM_2OTHER
MEM_B_DQS_0	*	*	MEM_2OTHER
MEM_B_DQS_1	*	*	MEM_2OTHER
MEM_B_DQS_2	*	*	MEM_2OTHER
MEM_B_DQS_3	*	*	MEM_2OTHER
MEM_B_DQS_4	*	*	MEM_2OTHER
MEM_B_DQS_5	*	*	MEM_2OTHER
MEM_B_DQS_6	*	*	MEM_2OTHER
MEM_B_DQS_7	*	*	MEM_2OTHER

MEM_A_DATA_0	*	*	MEM_2OTHER
MEM_A_DATA_1	*	*	MEM_2OTHER

MEM_A_DATA_2	*	*	MEM_2OTHER
MEM_A_DATA_3	*	*	MEM_2OTHER
MEM_A_DATA_4	*	*	MEM_2OTHER
MEM_A_DATA_5	*	*	MEM_2OTHER

MEM_A_DATA_6	*	*	MEM_2OTHER
MEM_A_DATA_7	*	*	MEM_2OTHER
MEM_B_DATA_0	*	*	MEM_2OTHER
MEM_B_DATA_1	*	*	MEM_2OTHER

MEM_B_DATA_2	*	*	MEM_2OTHER
MEM_B_DATA_3	*	*	MEM_2OTHER
MEM_B_DATA_4	*	*	MEM_2OTHER
MEM_B_DATA_5	*	*	MEM_2OTHER

MEM_B_DATA_6	*	*	MEM_2OTHER
MEM_B_DATA_7	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER

MEM_CLK	*	*	MEM_2OTHER
---------	---	---	------------

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DATA_0	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_1	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_2	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_3	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_4	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_5	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_6	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_7	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_0	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_1	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_2	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_3	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_4	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_5	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_6	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_7	MEM_*_DATA_*	*	MEM_2OTHERMEM

Memory Net Properties


ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
MEM_A_CLK0	MEM_70D	MEM_CLK	MEM A CLK P<0>	7 20 24
MEM_A_CLK0	MEM_70D	MEM_CLK	MEM A CLK N<0>	7 20 24
MEM_A_CLK1	MEM_70D	MEM_CLK	MEM A CLK P<1>	7 21 24
MEM_A_CLK1	MEM_70D	MEM_CLK	MEM A CLK N<1>	7 21 24
MEM_A_CTRL	MEM_40S	MEM_CTRL	MEM A CS_L<1..0>	7 20 21 24
MEM_A_CTRL	MEM_40S	MEM_CTRL	MEM A ODT<0>	7 20 21 24 61
MEM_A_CKE0	MEM_40S	MEM_CMD	MEM A CKE<1..0>	7 20 24
MEM_A_CKE1	MEM_40S	MEM_CMD	MEM A CKE<3..2>	7 21 24
MEM_A_CMD0	MEM_40S	MEM_CMD	MEM A CAA<9..0>	7 20 24 61
MEM_A_CMD1	MEM_40S	MEM_CMD	MEM A CAB<9..0>	7 21 24 61
MEM_A_DQ_BYTE0	MEM_40S	MEM_A_DATA_0	MEM A DQ<7..0>	7 61
MEM_A_DQ_BYTE1	MEM_40S	MEM_A_DATA_1	MEM A DQ<15..8>	7 61
MEM_A_DQ_BYTE2	MEM_40S	MEM_A_DATA_2	MEM A DQ<23..16>	7 61
MEM_A_DQ_BYTE3	MEM_40S	MEM_A_DATA_3	MEM A DQ<31..24>	7 61
MEM_A_DQ_BYTE4	MEM_40S	MEM_A_DATA_4	MEM A DQ<39..32>	7 21 61
MEM_A_DQ_BYTE5	MEM_40S	MEM_A_DATA_5	MEM A DQ<47..40>	7 61
MEM_A_DQ_BYTE6	MEM_40S	MEM_A_DATA_6	MEM A DQ<55..48>	7 61
MEM_A_DQ_BYTE7	MEM_40S	MEM_A_DATA_7	MEM A DQ<63..56>	7 61
MEM_A_DQS0	MEM_70D	MEM_A_DQS_0	MEM A DQS P<0>	7 61
MEM_A_DQS0	MEM_70D	MEM_A_DQS_0	MEM A DQS N<0>	7 61
MEM_A_DQS1	MEM_70D	MEM_A_DQS_1	MEM A DQS P<1>	7 61
MEM_A_DQS1	MEM_70D	MEM_A_DQS_1	MEM A DQS N<1>	7 61
MEM_A_DQS2	MEM_70D	MEM_A_DQS_2	MEM A DQS P<2>	7 61
MEM_A_DQS2	MEM_70D	MEM_A_DQS_2	MEM A DQS N<2>	7 61
MEM_A_DQS3	MEM_70D	MEM_A_DQS_3	MEM A DQS P<3>	7 61
MEM_A_DQS3	MEM_70D	MEM_A_DQS_3	MEM A DQS N<3>	7 61
MEM_A_DQS4	MEM_70D	MEM_A_DQS_4	MEM A DQS P<4>	7 61
MEM_A_DQS4	MEM_70D	MEM_A_DQS_4	MEM A DQS N<4>	7 61
MEM_A_DQS5	MEM_70D	MEM_A_DQS_5	MEM A DQS P<5>	7 61
MEM_A_DQS5	MEM_70D	MEM_A_DQS_5	MEM A DQS N<5>	7 61
MEM_A_DQS6	MEM_70D	MEM_A_DQS_6	MEM A DQS P<6>	7 21 61
MEM_A_DQS6	MEM_70D	MEM_A_DQS_6	MEM A DQS N<6>	7 21 61
MEM_A_DQS7	MEM_70D	MEM_A_DQS_7	MEM A DQS P<7>	7 61
MEM_A_DQS7	MEM_70D	MEM_A_DQS_7	MEM A DQS N<7>	7 61
MEM_B_CLK0	MEM_70D	MEM_CLK	MEM B CLK P<0>	7 22 24
MEM_B_CLK0	MEM_70D	MEM_CLK	MEM B CLK N<0>	7 22 24
MEM_B_CLK1	MEM_70D	MEM_CLK	MEM B CLK P<1>	7 23 24
MEM_B_CLK1	MEM_70D	MEM_CLK	MEM B CLK N<1>	7 23 24
MEM_B_CTRL	MEM_40S	MEM_CTRL	MEM B CS_L<1..0>	7 22 23 24
MEM_B_CTRL	MEM_40S	MEM_CTRL	MEM B ODT<0>	7 22 23 24 61
MEM_B_CKE0	MEM_40S	MEM_CMD	MEM B CKE<1..0>	7 22 24
MEM_B_CKE1	MEM_40S	MEM_CMD	MEM B CKE<3..2>	7 23 24
MEM_B_CMD0	MEM_40S	MEM_CMD	MEM B CAA<9..0>	7 22 24 61
MEM_B_CMD1	MEM_40S	MEM_CMD	MEM B CAB<9..0>	7 23 24 61
MEM_B_DQ_BYTE0	MEM_40S	MEM_B_DATA_0	MEM B DQ<7..0>	7 61
MEM_B_DQ_BYTE1	MEM_40S	MEM_B_DATA_1	MEM B DQ<15..8>	7 61
MEM_B_DQ_BYTE2	MEM_40S	MEM_B_DATA_2	MEM B DQ<23..16>	7 61
MEM_B_DQ_BYTE3	MEM_40S	MEM_B_DATA_3	MEM B DQ<31..24>	7 61
MEM_B_DQ_BYTE4	MEM_40S	MEM_B_DATA_4	MEM B DQ<39..32>	7 23 61
MEM_B_DQ_BYTE5	MEM_40S	MEM_B_DATA_5	MEM B DQ<47..40>	7 61
MEM_B_DQ_BYTE6	MEM_40S	MEM_B_DATA_6	MEM B DQ<55..48>	7 61
MEM_B_DQ_BYTE7	MEM_40S	MEM_B_DATA_7	MEM B DQ<63..56>	7 61
MEM_B_DQS0	MEM_70D	MEM_B_DQS_0	MEM B DQS P<0>	7 61
MEM_B_DQS0	MEM_70D	MEM_B_DQS_0	MEM B DQS N<0>	7 61
MEM_B_DQS1	MEM_70D	MEM_B_DQS_1	MEM B DQS P<1>	7 61
MEM_B_DQS1	MEM_70D	MEM_B_DQS_1	MEM B DQS N<1>	7 61
MEM_B_DQS2	MEM_70D	MEM_B_DQS_2	MEM B DQS P<2>	7 61
MEM_B_DQS2	MEM_70D	MEM_B_DQS_2	MEM B DQS N<2>	7 61
MEM_B_DQS3	MEM_70D	MEM_B_DQS_3	MEM B DQS P<3>	7 61
MEM_B_DQS3	MEM_70D	MEM_B_DQS_3	MEM B DQS N<3>	7 61
MEM_B_DQS4	MEM_70D	MEM_B_DQS_4	MEM B DQS P<4>	7 61
MEM_B_DQS4	MEM_70D	MEM_B_DQS_4	MEM B DQS N<4>	7 61
MEM_B_DQS5	MEM_70D	MEM_B_DQS_5	MEM B DQS P<5>	7 61
MEM_B_DQS5	MEM_70D	MEM_B_DQS_5	MEM B DQS N<5>	7 61
MEM_B_DQS6	MEM_70D	MEM_B_DQS_6	MEM B DQS P<6>	7 23 61
MEM_B_DQS6	MEM_70D	MEM_B_DQS_6	MEM B DQS N<6>	7 23 61
MEM_B_DQS7	MEM_70D	MEM_B_DQS_7	MEM B DQS P<7>	7 61
MEM_B_DQS7	MEM_70D	MEM_B_DQS_7	MEM B DQS N<7>	7 61
		MEM_PWR	PP1V2_S3	17 19 20 21 22 23 40
		MEM_PWR	PP0V6_S3 MEM VREFCA A	18 19 20 21
		MEM_PWR	PP0V6_S3 MEM VREFDO A	18 19 20 21
		MEM_PWR	PP0V6_S3 MEM VREFCA B	18 19 22 23
		MEM_PWR	PP0V6_S3 MEM VREFDO B	18 19 22 23

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Memory Constraints

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MIPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP
MIPI_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
MIPI_2OTHER	*	=4X_DIELECTRIC	?
MIPI_2CLK	*	=6X_DIELECTRIC	?
MIPICLK_2OTHER	*	=7X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MIPI_DATA	*	*	MIPI_2OTHER
MIPI_DATA	CLK_MIPI	*	MIPI_2CLK
CLK_MIPI	*	*	MIPICLK_2OTHER

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP
S2_MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
S2_MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
S2_DATA2SELF	*	=2x_DIELECTRIC	?
S2_DQS2OWNDATA	*	=2x_DIELECTRIC	?
S2_CMD2CMD	*	=2x_DIELECTRIC	?
S2_CMD2CTRL	*	=2x_DIELECTRIC	?
S2_CTRL2CTRL	*	=2x_DIELECTRIC	?
S2_2OTHERMEM	*	=4x_DIELECTRIC	?
S2MEM_2PWR	*	=2x_DIELECTRIC	?
S2MEM_2GND	*	=2x_DIELECTRIC	?
S2MEM_2OTHER	*	=6x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
S2_DATA2SELF	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_DQS2OWNDATA	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CMD2CMD	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CMD2CTRL	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CTRL2CTRL	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_2OTHERMEM	TOP,BOTTOM	=6x_DIELECTRIC	?
S2MEM_2PWR	TOP,BOTTOM	=4x_DIELECTRIC	?
S2MEM_2GND	TOP,BOTTOM	=4x_DIELECTRIC	?
S2MEM_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DATA*	*	*	S2MEM_2OTHER
S2_MEM_DQS*	*	*	S2MEM_2OTHER
S2_MEM_CMD	*	*	S2MEM_2OTHER
S2_MEM_CTRL	*	*	S2MEM_2OTHER
S2_MEM_CLK	*	*	S2MEM_2OTHER
S2_MEM_DATA*	=SAME	*	S2_DATA2SELF
S2_MEM_CMD	S2_MEM_CMD	*	S2_CMD2CMD
S2_MEM_CMD	S2_MEM_CTRL	*	S2_CMD2CTRL
S2_MEM_CTRL	S2_MEM_CTRL	*	S2_CTRL2CTRL
S2_MEM_*	S2_MEM_*	*	S2_2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DQS1	S2_MEM_DATA1	*	S2_DQS2OWNDATA
S2_MEM_DQS0	S2_MEM_DATA0	*	S2_DQS2OWNDATA

Memory to Power Spacing


NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_PWR	S2_MEM_*	*	S2MEM_2PWR
S2_MEM_PWR	*	*	DEFAULT

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	S2_MEM_*	*	S2MEM_2GND

Camera Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM_CAM_CLK_P	31 32
S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM_CAM_CLK_N	31 32
S2_MEM_CNTRL	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CKE	31 32
S2_MEM_CNTRL	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CS_L	31 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_ODT	32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CAS_L	31 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_RAS_L	31 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_WE_L	31 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<0>	31 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<1>	31 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<2>	31 32
S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM_CAM_DQS_P<0>	31 32
S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM_CAM_DQS_N<0>	31 32
S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM_CAM_DQS_P<1>	31 32
S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM_CAM_DQS_N<1>	31 32
S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM_CAM_DM<0>	31 32
S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM_CAM_DM<1>	31 32
S2_MEM_A	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_A<14..0>	31 32
S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM_CAM_DQ<7..0>	31 32
S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM_CAM_DQ<15..8>	31 32
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_P	31 32
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_N	31 32
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_CONN_P	32 62
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_CONN_N	32 62
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_P	31 32
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_N	31 32
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_CONN_P	32 62
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_CONN_N	32 62
		S2_MEM_PWR	PP1V35_CAM	31 32
		S2_MEM_PWR	PP0V675_CAM_VREF	31 32
		S2_MEM_PWR	PP0V675_MEM_CAM_VREFCA	32
		S2_MEM_PWR	PP0V675_MEM_CAM_VREFDQ	32


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